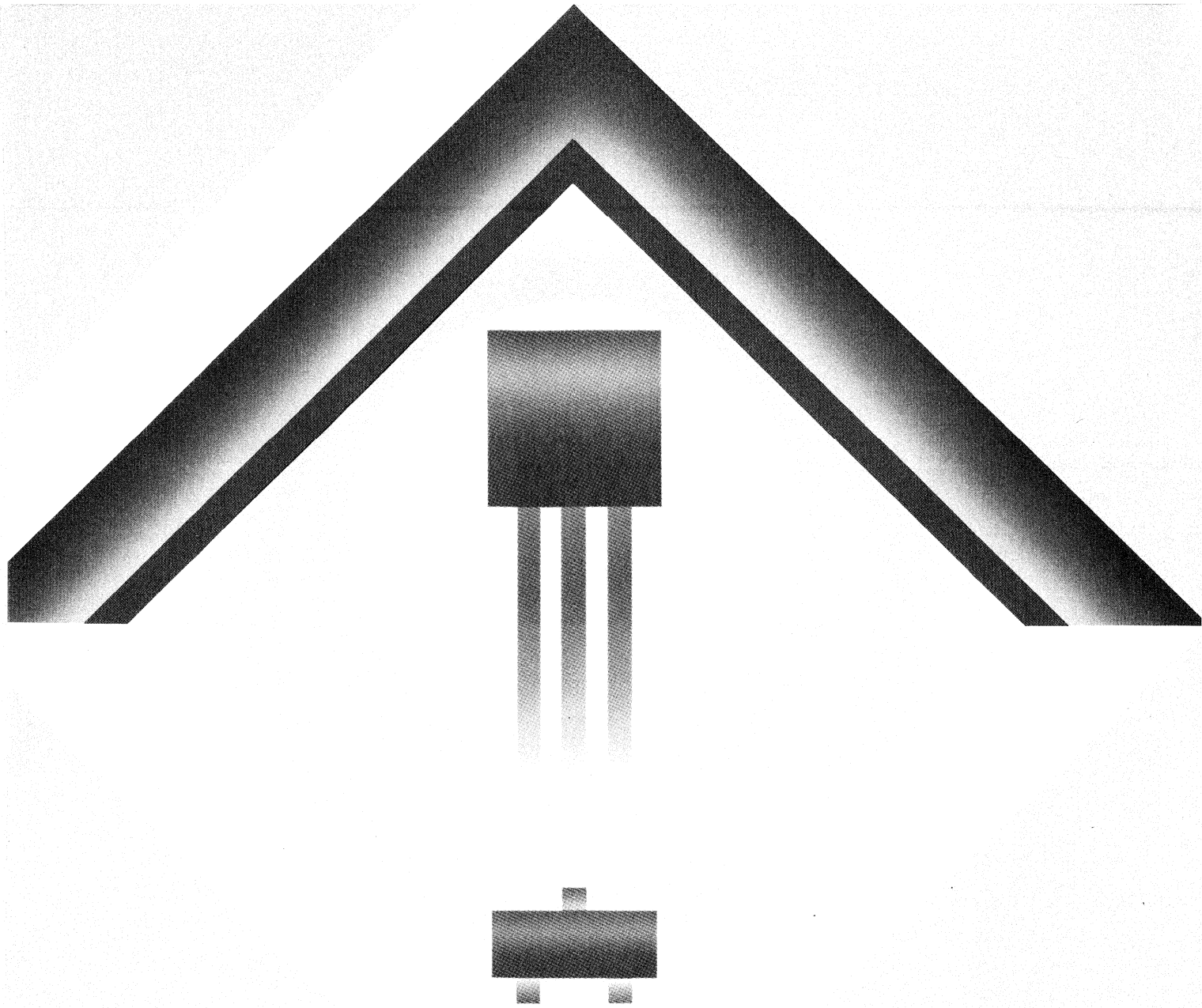


Transistors

6240-14-1E

ITT Semiconductors

ITT
Semiconductors

Transistors

Total Product Range
for Consumer Applications
and Professional Electronics

Manual 1991

Printed in Germany · Imprimé dans la République Fédérale d'Allemagne by Rombach GmbH Druck- und Verlagshaus, Freiburg i. Br.

Edition 1991/2 · Order No. 6240-14-1E

Page	Contents

Alphabetic Index of Types

NPN AF transistors for high-quality AF and DC amplifiers

in plastic case 10D3 (≈ TO-92)

BC413, BC414, BC549, BC550

in plastic case 23A3 resp. TO-236

BC849, BC850

NPN AF general purpose transistors for switching and amplifier applications

in plastic case 10D3 (≈ TO-92)

BC170, BC337, BC338, BC546 ... BC548, JC500, JC501

in plastic case 23A3 resp. TO-236

BC817, BC818, BC846, BC847, BC848, BCW60, BCX70

NPN AF transistors for high voltage drivers and output stages

in plastic case 10D3 (≈ TO-92)

BC445, BC447, BC449

PNP AF transistors for high-quality AF and DC amplifiers

in plastic case 10D3 (≈ TO-92)

BC415, BC416, BC559, BC560

in plastic case 23A3 resp. TO-236

BC859, BC860

PNP AF general purpose transistors for switching and amplifier applications

in plastic case 10D3 (≈ TO-92)

BC250, BC327, BC328, BC556 ... BC558, JA100, JA101

in plastic case 23A3 resp. TO-236

BC807, BC808, BC856, BC857, BC858, BCW61, BCX71

PNP transistors for high voltage drivers and output stages

in plastic case 10D3 (≈ TO-92)

BC446, BC448, BC450

VMOS Transistors

in plastic case 10D3 (≈ TO-92)

BS107, BS108, BS112, BS170, BS189, BS192, BS208, BS212, BS250

Technical Information

Index of Symbols

b	Imaginary part of y-Parameters
b_f	Imaginary part of forward transconductance y_f
b_i	Imaginary part of input admittance y_i
b_o	Imaginary part of output admittance y_o
b_r	Imaginary part of reverse transconductance y_r
B	Base connection
B_G	Imaginary part of generator (source) impedance
C	Capacitance; junction capacitance; collector connection
C_i	Input capacitance ($b_i/2\,\pi\,f$)
C_o	Output capacitance ($b_o/2\,\pi\,f$)
C_{CBO}	Collector base capacitance (open emitter)
C_{EBO}	Emitter base capacitance (open collector)
C_{iss}	Input capacitance
C_r	Feedback capacitance ($b_r/2\,\pi\,f$)
E	Emitter connection
f	Frequency
f_T	Gain bandwith product
F	Noise figure
F_c	Noise figure in mixer stages
g	Real part of y-parameters
g_f	Real part of forward transconductance y_f
g_i	Real part of input admittance y_i
g_m	Forward transconductance
g_o	Real part of output admittance y_o
g_r	Real part of reverse transconductance y_r
g_s	Generator conductance
G_C	Current gain
G_P	Power gain
$G_{P\,av}$	Available power gain
$G_{P\,max}$	Max. available power gain
G_V	Voltage gain
h	Parameters of h- (hybrid) matrix
h_f	Small signal current gain
h_i	Input impedance
h_o	Output admittance
h_r	Reverse voltage transfer ratio
h_{FE}	DC current gain, common emitter
I_B	Base current
I_{BM}	Peak base current
I_{B1}	Turn-on current
I_{B2}	Turn-off current
I_C	Collector current
I_{CAV}	Average collector current
I_{CBO}	Collector base cutoff current (open emitter)
I_{CEO}	Collector emitter cutoff current (open base)
I_{CER}	Collector emitter cutoff current (specified resistance between base and emitter)
I_{CES}	Collector emitter cutoff current (base short-circuited to emitter)
I_{CEV}	Collector emitter cutoff current (specified voltage between base and emitter)
I_{CM}	Peak collector current
I_D	Drain current
I_{DSS}	Drain cutoff current
I_E	Emitter current
I_{EBO}	Emitter base cutoff current (open collector)
I_{GSS}	Gate-body leakage current
K_V	Thermal resistance correction factor
P_{tot}	Power dissipation
P_D	Continuous power dissipation
P_l	Pulse power dissipation
$r_{b'} \cdot C_c$	Collector base time constant
$r_{DS\,(ON)}$	Drain source on resistance
r_{thA}	Pulse thermal resistance junction to ambient air
r_{thC}	Pulse thermal resistance junction to case
R	Resistance; resistor
R_{BE}	Resistance between base and emitter
R_G	Generator impedance; source impedance
$R_{G\,opt}$	Optimum (matched) generator resistance
R_L	Load resistance
$R_{L\,opt}$	Optimum (matched) load resistance
R_S	Series resistance
R_{th}	Thermal resistance
R_{thA}	Thermal resistance junction to ambient air
R_{thC}	Thermal resistance junction to case resp. mounting base
$R_{thC/S}$	Thermal resistance case or mounting base to heat sink
R_{thS}	Thermal resistance heat sink to ambient air
t	Time
t_d	Dealy time
t_f	Fall time
t_{off}	Turn-off time ($t_s + t_f$)
t_{on}	Turn-on time ($t_d + t_r$)
t_p	Pulse duration
t_{pd}	Propagation delay time
t_r	Rise time
t_s	Storage time
t_{total}	Total switching time ($t_{on} + t_{off}$)
T	Temperature; duration of one period
T_{amb}	Ambient temperature
T_j	Junction temperature
T_C	Case temperature
T_S	Storage temperature
T_{SB}	Temperature of substrate backside

V	Voltage
V_{BB}	Base supply voltage
V_{BE}	Base emitter voltage
$V_{BE\ sat}$	Base emitter saturation voltage
$V_{(BR)CBO}$	Collector base breakdown voltage (open emitter)
$V_{(BR)CEO}$	Collector emitter breakdown voltage (open base)
$V_{(BR)CER}$	Collector emitter breakdown voltage (specified resistance between base and emitter)
$V_{(BR)CES}$	Collector emitter breakdown voltage (emitter short-circuited to base)
V_{DGS}	Drain gate voltage
V_{DSS}	Drain source voltage
$V_{(BR)DSS}$	Drain source breakdown voltage
$V_{(BR)EBO}$	Emitter base breakdown voltage (open collector)
V_{CB}	Collector base voltage
V_{CBO}	Collector base voltage (open emitter)
V_{CC}	Collector supply voltage
V_{CE}	Collector emitter voltage
V_{CEO}	Collector emitter voltage (open base)
V_{CER}	Collector emitter voltage (specified resistance between base and emitter)
V_{CES}	Collector emitter voltage (emitter short-circuited to base)
$V_{CE\ sat}$	Collector emitter saturation voltage
V_{CEV}	Collector emitter voltage (specified voltage between base and emitter)
V_{EBO}	Emitter base voltage (open collector)
V_{EE}	Emitter supply voltage
$V_{GS(TO)}$	Gate threshold voltage
V_i	Input voltage
V_o	Output voltage
y	Parameters of y- (admittance) matrix
y_f	Forward transconductance
y_i	Input admittance
y_o	Output admittance
y_r	Reverse transconductance
y_s	Generator admittance
Z_1	Input impedance
Z_2	Output impedance
φ	Phase angle of y-parameters
τ_s	Storage time constant
ν	Duty cycle (t_p/T)

Technical Information

Characteristics and Maximum Ratings

The electrical performance of a semiconductor device is usually expressed in terms of its characteristics and maximum ratings.

Characteristics are those which can be measured by use of suitable measuring instruments and circuits, and provide information on the performance of the device under specified operating conditions (at a given bias, for example). Depending on requirements, they are quoted either as typical (Typ.) values or guaranteed (Min., Max.) values.

Typical values are expressed as figures or as one or more curves, and are subject to spreads. Occasionally a typical curve is accompanied by another curve, this being a 95%, or, in a few cases, a maximum spread limit curve.

Maximum Ratings give the values which cannot be exceeded without risk of damage to the device. Changes in supply voltage and in the tolerances of other components in the circuit must also be taken into consideration. No single maximum rating should ever be exceeded, even when the device is operated well within the other maximum ratings. The inclusion of the word "admissible" in a title means that the associated curve defines the maximum ratings.

An exception to this rule are data on collector current. The collector current, quoted as one of the critical transistor values, is a maximum value recommended by the manufacturer which should be noted in connection with the other characteristics valid for this collector current (e. g. collector and saturation voltages, current gain etc.) when selecting a transistor. In certain cases, the quoted collector current may be exceeded without the transistor being destroyed. The absolute limit for the collector current is determined by the maximum admissible power dissipation of the transistor.

Assembly and Soldering Instructions

To prevent transistors from being damaged during mounting, observe the following points:

All semiconductor devices are extremely sensitive to their maximum admissible junction temperature being exceeded. When planning the layout of the equipment, the distance between heat sources and semiconductor elements should be sufficiently large.

Semiconductor elements may be mounted in any desired position.

From the experience gained in soldering semiconductor elements the following rules have emerged:

For transistors in plastic cases 10C3 and 10D3 the maximum soldering time is 8 s, at soldering temperatures between 230 and 260 °C. Here, the distance between soldered joint and case should be at least 4 mm. During soldering, the leads should not be subjected to mechanical stress.

For transistors in plastic case 23A3 the maximum soldering time is 5 sec., at a maximum soldering temperature of 240 °C.

Admissible Power Dissipation

The indicated maximum admissible junction temperature must not be exceeded because this could damage or cause the destruction of the transistor crystal. Since the user cannot measure this temperature, data sheets also reveal the maximum admissible power dissipation P_{tot} usually in the form of a derating curve (see diagram).

If power dissipation is kept within these limits the maximum junction temperature will not be exceeded. This can easily be checked by using the equation

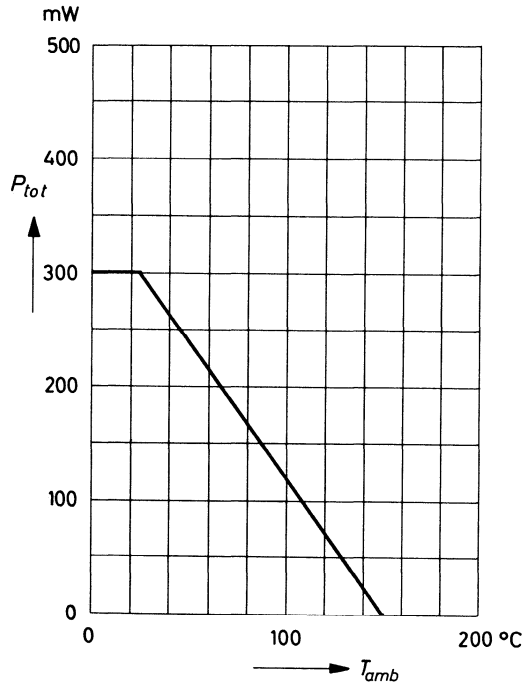
$T_j = T_{amb} + P_{tot} \cdot R_{th}$

For the thermal resistance R_{th} the junction to ambient thermal resistance R_{thA} is usually substituted in the case of small transistors (in the TO-18 or TO-92 package). In the case of power transistors (in the TO-202 or similar packages) which are usually mounted on a cooling fin or heat sink for the purpose of heat dissipation, the sum of the junction to case thermal resistance R_{thC} plus the heat sink to ambient thermal resistance R_{thS} plus – for more accurate calculations – the mounting surface to heat sink thermal resistance is substituted for the thermal resistance in this equation. In order to keep the mounting surface to heat sink thermal resistance low, a heat conducting compound (silicone grease) is to be applied to the mounting surface before the transistor is screwed on. If a mica insulation is used, the thermal resistance of the mica washer must be added which amounts to about 0,5 K/W.

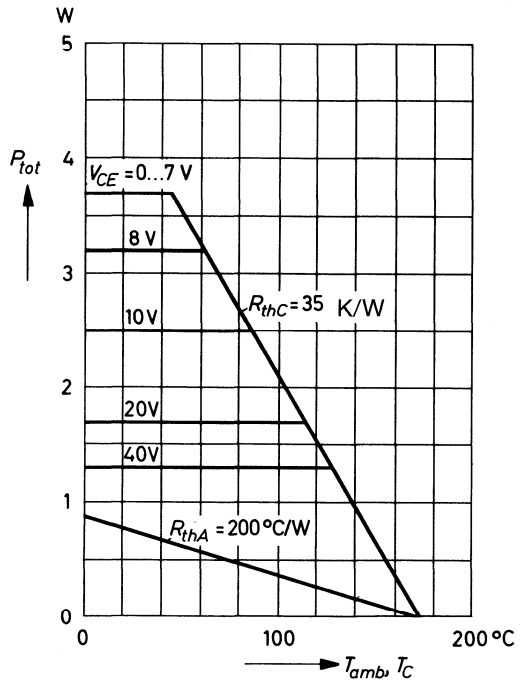
Directions for determining the thermal resistance R_{thS} for cooling fins can be found on page 13.

Since the distribution of heat in the transistor crystal is not uniform and depends on voltage and current, some transistors are accompanied by derating curves showing P_{tot} as a function of T_C and T_{amb} with the collector voltage V_{CE} as parameter (see diagram below).

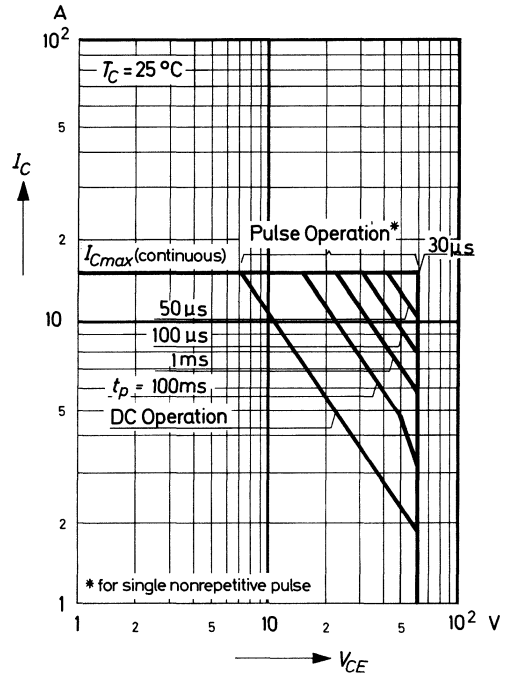
Admissible power dissipation versus ambient temperature



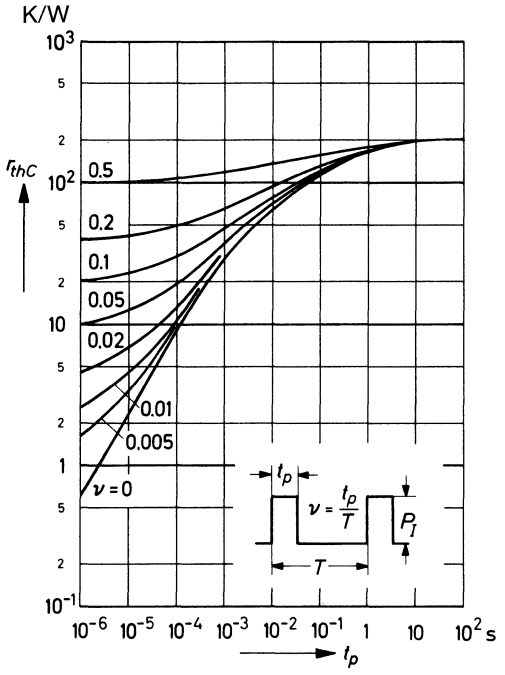
Admissible power dissipation versus temperature



Admissible collector current versus collector emitter voltage



Pulse thermal resistance versus pulse duration



For some power transistors the data sheets also contain a diagram giving "admissible collector current" or "permissible operating range" which gives further information on admissible power dissipation. One example is illustrated in the diagram left.

These diagrams are based on continuous power dissipation. However, pulse power dissipation may usually exceed continuous power dissipation. To ascertain maximum admissible pulse power dissipation P_I, reference is made to the pulse junction to case thermal resistance r_{thC} or the pulse junction to ambient thermal resistance r_{thA} whose value can be derived from the $r_{th} = f(t_p)$ diagram below.

Use the equation

$$T_j = T_{amb} + P_I \cdot r_{thA}$$

or, if the continuous power dissipation P_D is to be taken into consideration:

$$T_j = T_{amb} + P_D \cdot R_{thA} + P_I \cdot r_{thA}$$

If the transistor is mounted on a cooling fin then the equation becomes:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_I \cdot r_{thC}$$

wherein P_{tot} is the mean value of the pulse power dissipation P_I. Where continuous power dissipation must be considered in addition, the equation is expanded accordingly:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_D \cdot R_{thC} + P_I \cdot r_{thC}$$

wherein P_{tot} is the mean value of the total power dissipation.

The thermal resistance and pulse thermal resistance values derived from the data sheets apply without limitation only to small collector emitter voltages V_{CE}, between about 5 and 10 V. For higher voltages these thermal resistance values have to be multiplied by a correction factor K_V which has to be calculated from the previously mentioned derating curves. The admissible power dissipation $P_{tot\ max}$, applicable to low collector voltages, must be divided by the admissible power dissipation $P_{tot\ V}$ for the higher collector voltage V:

$$K_V = \frac{P_{tot\ max}}{P_{tot\ V}}$$

The complete equation for T_j then reads:

$$T_j = T_{amb} + P_{tot} \cdot R_{thS} + P_D \cdot K_V \cdot R_{thC} + P_I \cdot K_V \cdot r_{thC}$$

Heat Removal from Transistors

The operation of any semiconductor device involves the dissipation of power with a consequent rise in junction temperature. Because the maximum admissible junction temperature must be not exceeded, careful circuit design with due regard not only to the electrical, but also the thermal performance of a semiconductor circuit, is essential.

If the dissipated power is low, then sufficient heat is radiated from the surface of the case; if the dissipation is high, however, additional steps may have to be taken to promote this process by reducing the thermal resistance between the junction and the ambient air. This can be achieved either by pushing a star- or flag-shaped heat dissipator over the case, or by bolting the semiconductor device to a heat sink.

P, the power to be dissipated, T_j the junction temperature, and T_{amb}, the ambient temperature are related by the formula

$$P = \frac{T_j - T_{amb}}{R_{thA}} = \frac{T_j - T_{amb}}{R_{thC} + R_{thS}},$$

where R_{thA} is the total thermal resistance beween junction and ambient air. The total thermal resistance in turn comprises an internal thermal resistance R_{thC} between the junction and the mounting base, and an outer thermal resistance R_{thS} between the case and the surrounding air (or any other cooling medium). It should be noted that only the outer thermal resistance is affected by the design of the heat sink. To determine the size of the heat sink required to meet given operating conditions, proceed as follows: First calculate the outer thermal resistance by use of the formula

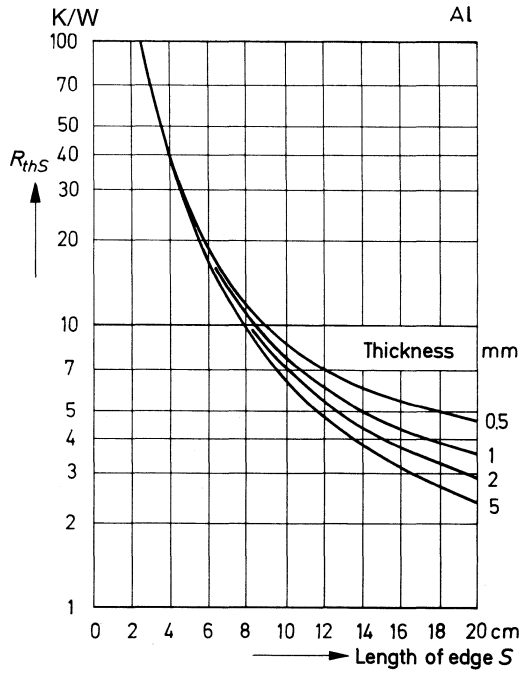
$$R_{thS} < \frac{T_j - T_{amb}}{P} - R_{thC}$$

and then, by use of the diagrams, determine the size of the heat sink which provides the calculated R_{thS}-value. To determine the maximum admissible device dissipation and ambient temperature limit for a given heat sink, proceed in the reverse order to that described above.

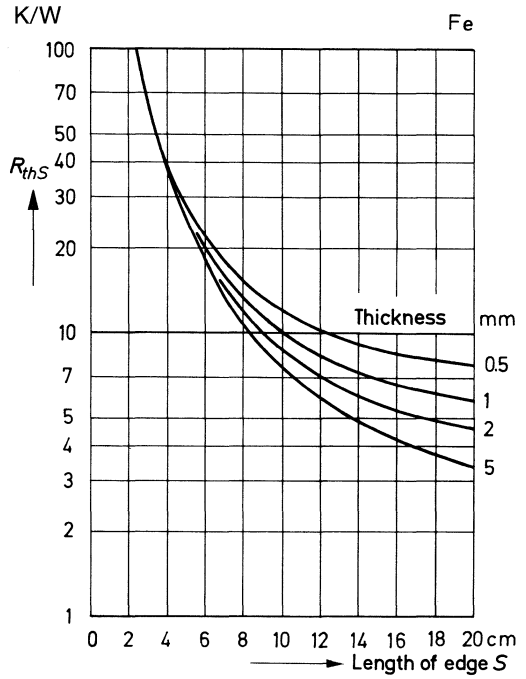
The calculations are based on the following assumptions: Use of a squareshaped heat sink without any finish, mounted in a vertical position; semiconductor device located in the centre of the sink; heat sink operated in still air and not subjected to any additional heat radiation. The calculated area should be increased by a factor of 1.3 if the sink is mounted horizontally, and can be reduced by a factor of approximately 0.7 if a black finish is used.

The curves give the thermal to ambient resistance of square vertical heat sinks as a function of side length. It is assumed that the heat is applied at the centre of the square.

Aluminium Cooling Fin

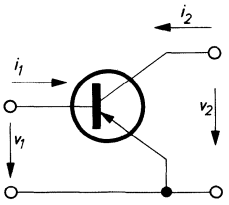


Steel Cooling Fin

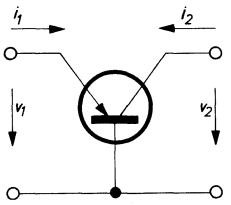


Basic Circuits

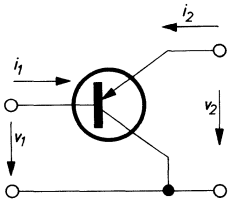
There are three basic transistor circuits. They are called according to that electrode (emitter, base, collector) which is common to both input and output circuit.



Common Emitter



Common Base



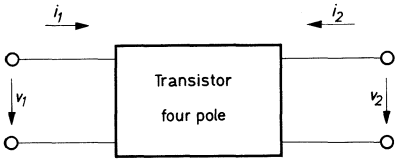
Common Collector

Properties of the three basic circuits:

	Common Emitter	Common Base	Common Collector
Input impedance	medium	small	high
Output impedance	medium	high	small
Current gain	high	less than 1	high
Upper frequency limit	low	high	low

Four-Pole-Symbols of h-Matrix

A transistor can be considered as an active four-pole network. When driven with small low-frequency signals its properties can be described by the four characteristic values of the h- (hybrid) matrix, which are assumed to be real.



$$v_1 = h_i \cdot i_1 + h_r \cdot v_2$$

$$i_2 = h_f \cdot i_1 + h_o \cdot v_2$$

If expressed this in matrix form we obtain:

$$\begin{pmatrix} v_1 \\ i_2 \end{pmatrix} = (h) \begin{pmatrix} i_1 \\ v_2 \end{pmatrix} \qquad (h) = \begin{pmatrix} h_i & h_r \\ h_f & h_o \end{pmatrix}$$

Explanation of h-Parameters

Input impedance (shorted output, $v_2 = 0$):

$$h_i = \frac{v_1}{i_1}$$

Reverse voltage transfer ratio (open input, $i_1 = 0$):

$$h_r = \frac{v_1}{v_2}$$

Small signal current gain (shorted output, $v_2 = 0$):

$$h_f = \frac{i_2}{i_1}$$

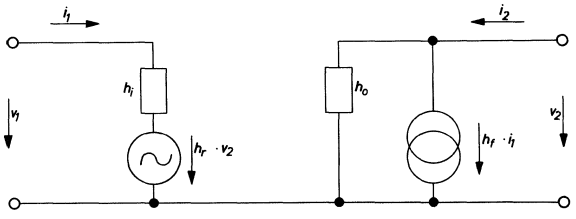
Output admittance (open input, $i_1 = 0$):

$$h_o = \frac{i_2}{v_2}$$

A frequently used abbreviation is the determinant:

$$\triangle h = h_i \cdot h_o - h_r \cdot h_f$$

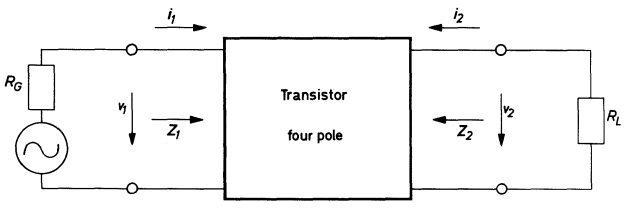
For all three basic circuit configurations the circuit illustrated below represents the equivalent four-pole circuit using h-parameters.



In the transistor data sheets the h-parameters are usually quoted for the common emitter configuration and for a given operating point (bias). The latter is determined by the collector voltage, the emitter or collector current and by the ambient temperature. For different operating points, correction factors are needed which can be gathered from the relevant curves. For common base or common collector transistor stage calculations, the appropriate h-parameters are ascertained from those of the common emitter configuration by using the following conversion formulas.

	Common Emitter	Common Base	Common Collector
Input impedance	h_{ie}	$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$
Reverse voltage transfer ratio	h_{re}	$h_{rb} = \frac{h_{ie} \cdot h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re}$
Small signal current gain	h_{fe}	$h_{fb} = -\frac{h_{fe}}{1 + h_{fe}}$	$-h_{fc} = 1 + h_{fe}$
Output admittance	h_{oe}	$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$

Calculation of a Transistor Stage



Input impedance

$$Z_1 = \frac{v_1}{i_1} = \frac{h_i + R_L \cdot \triangle h}{1 + h_o \cdot R_L}$$

Output impedance

$$Z_2 = \frac{v_2}{i_2} = \frac{h_i + R_G}{\triangle h + h_o \cdot R_G}$$

Current gain

$$G_C = \frac{i_2}{i_1} = \frac{h_f}{1 + h_o \cdot R_L}$$

Voltage gain

$$G_V = \frac{v_2}{v_1} = \frac{-h_f \cdot R_L}{h_i + R_L \cdot \triangle h}$$

Power gain

$$G_P = \frac{v_2 \cdot i_2}{v_1 \cdot i_1} = \frac{h_f^2 \cdot R_L}{(1 + h_o \cdot R_L)\,(h_i + R_L \cdot \triangle h)}$$

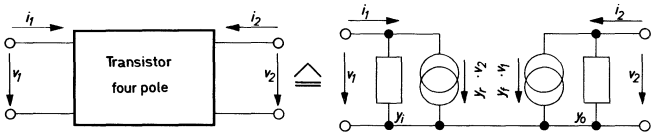
Max. available power gain, input and output matched with $R_{G\,opt}$ resp. $R_{L\,opt}$

$$G_{p\,max} = \left(\frac{h_f}{\sqrt{\triangle h} + \sqrt{h_i \cdot h_o}} \right)^2$$

$$R_{G\,opt} = \sqrt{\frac{h_i \cdot \triangle h}{h_o}} \qquad R_{L\,opt} = \sqrt{\frac{h_i}{h_o \cdot \triangle h}}$$

Four-Pole Symbols of y-Matrix

Whereas the network behaviour of low-frequency transistors could be described by using the h- (hybrid) matrix, the y- (admittance) matrix is usually employed for high frequency transistors.



$$i_1 = y_i \cdot v_1 + y_r \cdot v_2$$

$$i_2 = y_f \cdot v_1 + y_o \cdot v_2$$

In matrix form we obtain:

$$\left(\frac{i_2}{i_1} \right) = (y) \left(\frac{v_1}{v_2} \right) \qquad (y) = \begin{pmatrix} y_i & y_r \\ y_f & y_o \end{pmatrix}$$

The y-parameters are complex values which can be expressed as

$y_{ik} = g_{ik} + jb_{ik}$ with $b_{ik} = \omega C_{ik}$ or with $b_{ik} = -\frac{1}{\omega L_{ik}}$

Often, the following notation is expedient:

$y_{ik} = |\, y_{ik} \,| \exp j\varphi_{ik}$

By adding the suffix e, b, or c it is possible to indicate to which of the three basic circuit configurations the parameters are valid.

Explanation of y-Parameters

Input admittance (shorted output, $v_2 = 0$)

$$y_i = \frac{i_1}{v_1}$$

Reverse transconductance (shorted input, $v_1 = 0$)

$$y_r = \frac{i_1}{v_2}$$

Forward transconductance (shorted output, $v_2 = 0$)

$$y_f = \frac{i_2}{v_1}$$

Output admittance (shorted input, $v_1 = 0$)

$$y_o = \frac{i_2}{v_2}$$

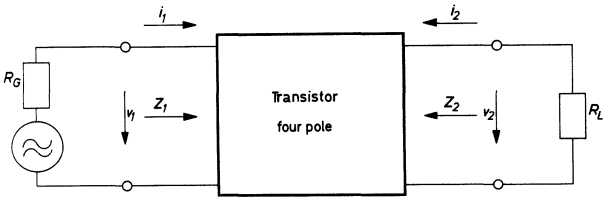
The determinant reads $\triangle y = y_i \cdot y_o - y_r \cdot y_f$

Conversion from y-Parameters to h-Parameters

$$h_i = \frac{1}{y_i} \qquad h_r = -\frac{y_r}{y_i} \qquad \triangle h = \frac{y_o}{y_i}$$

$$h_f = \frac{y_f}{y_i} \qquad h_o = \frac{\triangle y}{y_i}$$

Calculation of a Transistor Stage



Input impedance

$$Z_1 = \frac{v_1}{i_1} = \frac{1 + y_o \cdot R_L}{y_i + \triangle y \cdot R_L}$$

Output impedance

$$Z_2 = \frac{v_2}{i_2} = \frac{1 + y_i \cdot R_G}{y_o + \triangle y \cdot R_G}$$

Current gain

$$G_C = \frac{i_2}{i_1} = \frac{y_f}{y_i + \triangle y \cdot R_L}$$

Voltage gain

$$G_V = \frac{v_2}{v_1} = \frac{-y_f \cdot R_L}{1 + y_o \cdot R_L}$$

Power gain

$$G_P = \frac{v_2 \cdot i_2}{v_1 \cdot i_1} = \frac{|y_f|^2 \cdot R_L}{(1 + y_o \cdot R_L)\ (y_i + \triangle y \cdot R_L)}$$

Available power gain, input matched with $R_{G\ opt}$

$$G_{p\ av} = \frac{4 \cdot y_f^2 \cdot R_G \cdot R_L}{[(y_1 + \triangle y \cdot R_L) \cdot R_G + 1 + y_o \cdot R_L]^2}$$

Max. available power gain, input and output matched with $R_{G\ opt}$ resp. $R_{L\ opt}$

$$G_{P\ max} = \left(\frac{y_f}{\sqrt{\triangle y} + \sqrt{y_i \cdot y_o}} \right)^2$$

Max. available power gain will be attained if input and output are matched, where:

$$R_{L\ opt} = \sqrt{\frac{y_o}{y_i} \cdot \frac{1}{\triangle y}}$$

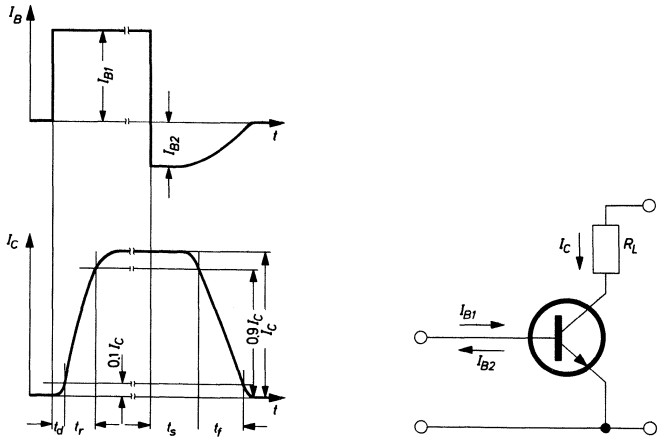
$$R_{G\ opt} = \sqrt{\frac{y_i}{y_o} \cdot \frac{1}{\triangle y}}$$

and:

$$\triangle y = y_i \cdot y_o - y_r \cdot y_f$$

Switching Times

Definitions for the various times which make up the total switching time can be gathered from the diagram below in which the switching characteristic of a transistor in common-emitter configuration is illustrated.

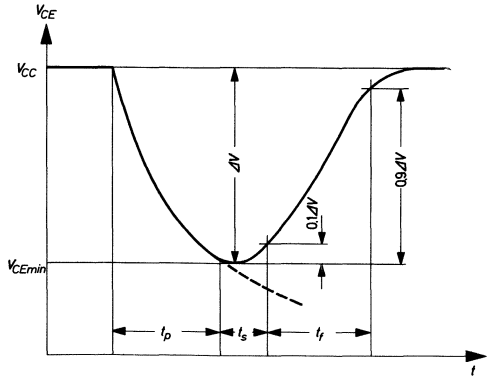


t_d	Delay time
t_r	Rise time
t_s	Storage time
t_f	Fall time
$t_{on} = t_d + t_r$	Turn-on time
$t_{off} = t_s + t_f$	Turn-off time

The duration of the switching times depends upon the transistor type and very much on the circuit arrangement.

With increasing saturation of the transistor the turn-on time decreases and the turn-off time increases. An increase of the turn-off current I_{B2} shortens the turn-off time.

The switching times depend on the duration of the turn-on pulse. It is only when the duration of this pulse is a multiple of the switching times that the latter remain constant. If the pulse is shorter, especially the storage time decreases. With a pulse duration in the region of the turn-on time the transistor is no longer fully saturated. The collector voltage then exhibits a characteristic such as is qualitatively represented in the diagram below.



DIN Standards (German)

The information contained in this book conforms, in the main, to the following German DIN Standards.

DIN 41785 Sheet 1 (10. 69)
Semiconductor devices, letter symbols on data sheets, general

DIN 41785 Part 2 (6. 76)
Semiconductor devices, letter symbols on data sheets for semiconductor devices for telecommunication

DIN 41791 Sheet 1 (9. 71)
Semiconductors for telecommunication, recommendations for data sheets, general

DIN 41791 Sheet 4 (3.74)
Semiconductor devices for telecommunication, recommendations for data sheets, low power signal transistors

DIN 41791 Sheet 6 (6.76)
Semiconductor devices for telecommunication, recommendations for data sheets, switching transistors

DIN 41791 Sheet 9 (4. 74)
Low power semiconductor devices; recommendations for data sheets; field-effect transistors

DIN 41854 (10.79)
Transistors, terms and definitions

DIN 41855 (10. 74)
Semiconductor devices, kinds of semiconductor devices, terms and definitions

DIN 41858 (11. 73)
Field-effect transistors, terms and definitions

DIN 41869 Sheet 1 (7.73)
Case 23A3 for semiconductor devices; main dimensions

DIN 41870 Sheet 1 (4. 69)
Cases for semiconductor devices and integrated circuits, short designations

DIN 41870 Part 2 (7.83)
Cases for semiconductor devices and integrated circuits, survey, terminal covering

DIN 41870 Part 4 (9.82)
Cases for semiconductor devices and integrated circuits; Cases 10B3 and 10D3 (IEC: 68)

Specifications for Quality

1. General

The outgoing quality of ITT's semiconductor devices is determined by the 100% testing of the guaranteed parameters with the most modern equipment. It is assured by means of a sampling system based on the laws of statistics covering all electrical and mechanical limit values.

The Quality is described by AQL-values (AQL = Acceptable Quality Level), which define the percentage of defectives in a batch, at or below which there is at least a 90% probability of the batch being accepted.

2. Defectives

Defectives are defined in terms of the maximal ratings and guaranteed characteristics of electrical and mechanical parameters. A device is considered defective if any one parameter does not lie within the limits quoted in the data-sheet. If an item has more than one defect, then this is counted as one defect only, i.e. a batch is assessed on the number of defective items and not on the number of defects. Defects are classified according to type and degree.

Type of defects:
a) Mechanical defects (case and leads)
b) Electrical defects

Degree of defects:
a) Catastrophic defects are those which preclude any use of the item
b) Limit defects are those which allow restricted use of the item

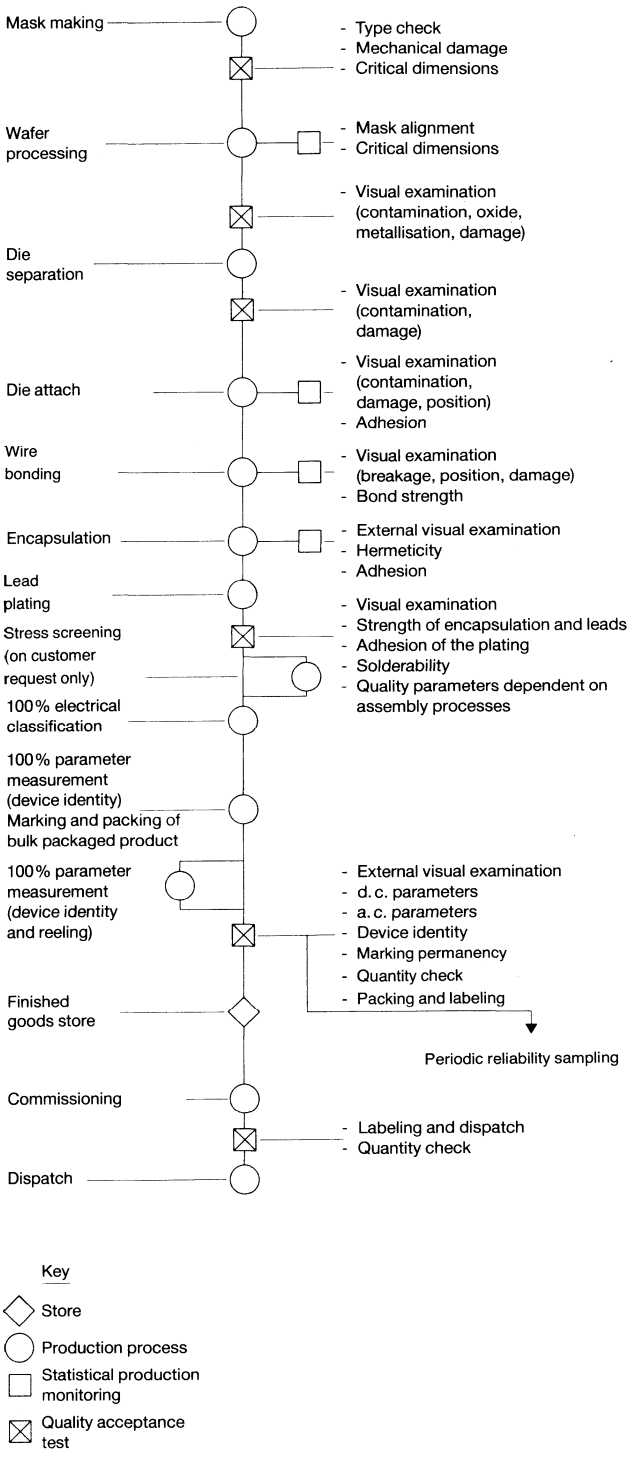
3. AQL (Acceptable Quality Level) Values

The group AQL values for the stated failure groups are given below. The AQL values apply to the sum of all defectives within the group.

Defectives:		
Mechanical:	Catastrophic defectives	0.065
	Limit defectives	0.25
Electrical:	Catastrophic defectives	0.025
	Limit defectives	0.065

The tests carried out by the manufacturer are designed so as to obviate the need for any incoming inspection by the user. If, however, a user wishes to carry out an incoming inspection, then this should be done on a sample basis, as laid down in the internationally accepted MIL-STD 105 D (DIN 40080) specifications.

Quality control during manufacture Transistors



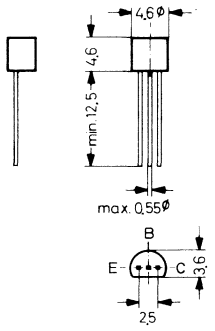
NPN Silicon Transistors

BC170

NPN Silicon Planar Transistor
for switching and amplifier applications

The transistor is subdivided into three groups, A, B and C, according to its DC current gain.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector Base Voltage	V_{CBO}	20	V
Collector Emitter Voltage	V_{CEO}	20	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	300[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 to +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current gain						
at V_{CE} = 1 V, I_C = 1 mA	**Current Gain Group A**	h_{FE}	35	–	100	–
	B	h_{FE}	80	–	250	–
	C	h_{FE}	200	–	600	–
at V_{CE} = 1 V, I_C = 30 mA	**Current Gain Group A**	h_{FE}	30	–	–	–
	B	h_{FE}	60	–	–	–
	C	h_{FE}	150	–	–	–
Collector Saturation Voltage						
at I_C = 1 mA, I_B = 0.1 mA		V_{CEsat}	–	–	0.25	V
at I_C = 30 mA, I_B = 3 mA		V_{CEsat}	–	–	0.4	V
Base Saturation Voltage						
at I_C = 1 mA, I_B = 0.1 mA		V_{BEsat}	–	–	0.7	V

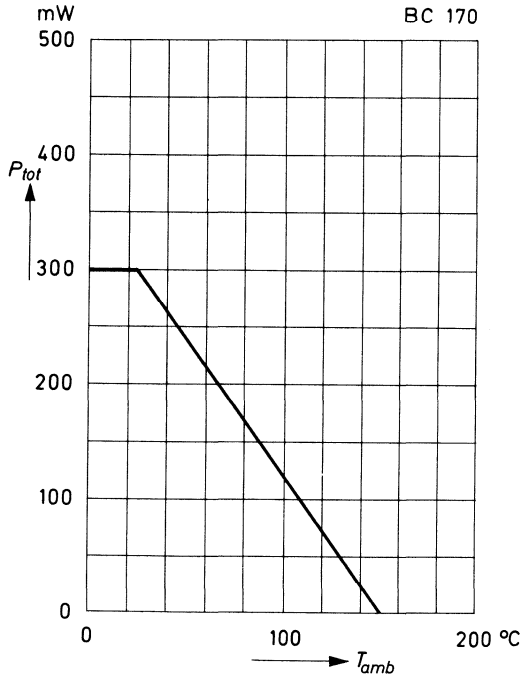
Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Collector Cutoff Current at V_{CB} = 15 V	I_{CBO}	–	–	0.1	μA
Emitter Cutoff Current at V_{EB} = 3.8 V	I_{EBO}	–	–	0.1	μA
Collector Base Capacitance at V_{CBO} = 10 V, f = 1 MHz	C_{CBO}	–	4	–	pF
Emitter Base Capacitance at V_{EBO} = 0.5 V, f = 1 MHz	C_{EBO}	–	12	–	pF
Gain Bandwith Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Noise Figure at V_{CE} = 5 V, I_C = 0.2 mA, R_G = 2 kΩ, f = 1 kHz, △f = 200 Hz	F	–	–	10	dB
Thermal Resistance Junction to Ambient	R_{thA}	–	–	420[1)]	K/W

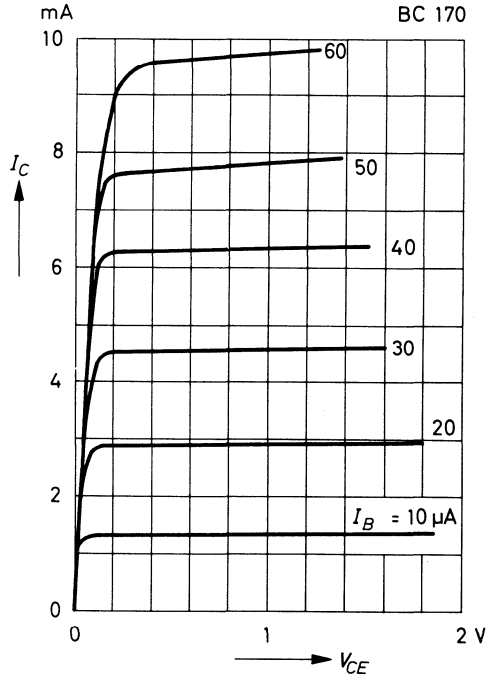
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



Common emitter collector characteristics

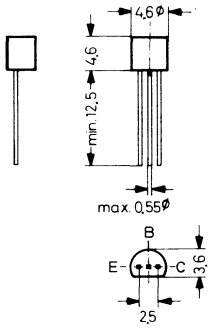


BC337, BC338

NPN Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups -16, -25 and -40, according to their DC current gain. As complementary types the PNP transistors BC327 and BC328 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC337** **BC338**	V_{CES} V_{CES}	50 30	V V
Collector Emitter Voltage	**BC337** **BC338**	V_{CEO} V_{CEO}	45 25	V V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1	A
Base Current		I_B	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 to +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

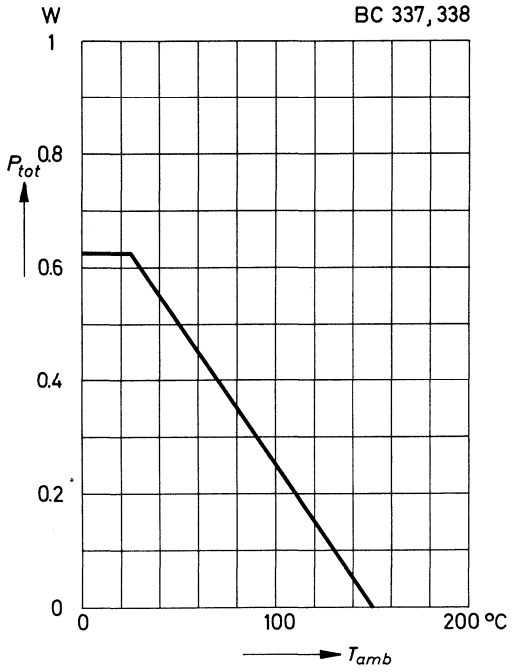
Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain						
at V_{CE} = 1 V, I_C = 100 mA	**BC337, BC338**	h_{FE}	100	–	630	–
	Current Gain Group 16	h_{FE}	100	160	250	–
	25	h_{FE}	160	250	400	–
	40	h_{FE}	250	400	630	–
at V_{CE} = 1 V, I_C = 300 mA	**BC337, BC338**	h_{FE}	60	–	–	–
	Current Gain Group 16	h_{FE}	60	130	–	–
	25	h_{FE}	100	200	–	–
	40	h_{FE}	170	320	–	–
Collector Cutoff Current						
at V_{CE} = 25 V	**BC338**	I_{CES}	–	2	100	nA
at V_{CE} = 45 V	**BC337**	I_{CES}	–	2	100	nA
at V_{CE} = 25 V, T_{amb} = 125 °C	**BC338**	I_{CES}	–	–	10	μA
at V_{CE} = 45 V, T_{amb} = 125 °C	**BC337**	I_{CES}	–	–	10	μA
Collector Emitter Breakdown Voltage						
at I_C = 10 mA	**BC338**	$V_{(BR)CEO}$	20	–	–	V
	BC337	$V_{(BR)CEO}$	45	–	–	V
Collector Emitter Breakdown Voltage						
at I_C = 0.1 mA	**BC338**	$V_{(BR)CES}$	30	–	–	V
	BC337	$V_{(BR)CES}$	50	–	–	V
Emitter Base Breakdown Voltage at I_E = 0.1 mA		$V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA		V_{CEsat}	–	–	0.7	V
Base Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA		V_{BE}	–	–	1.2	V
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz		f_T	–	100	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	12	–	pF
Thermal Resistance Junction to Ambient		R_{thA}	–	–	200[1]	K/W

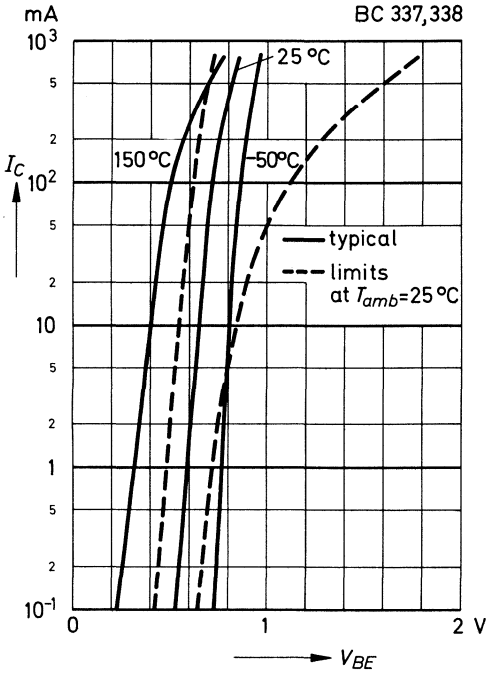
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

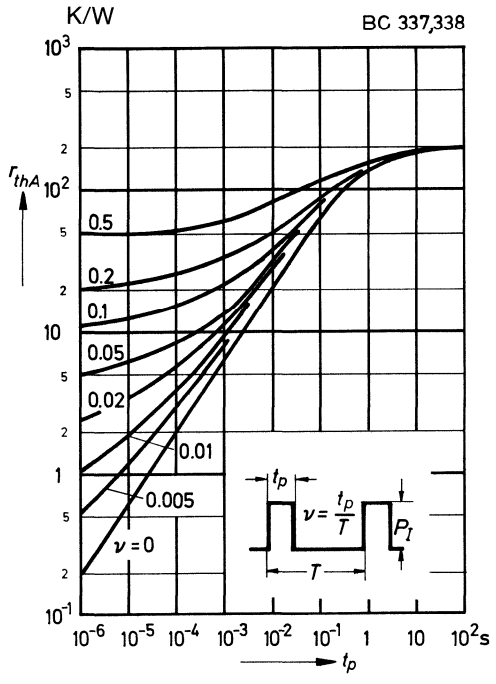


Collector current versus base emitter voltage

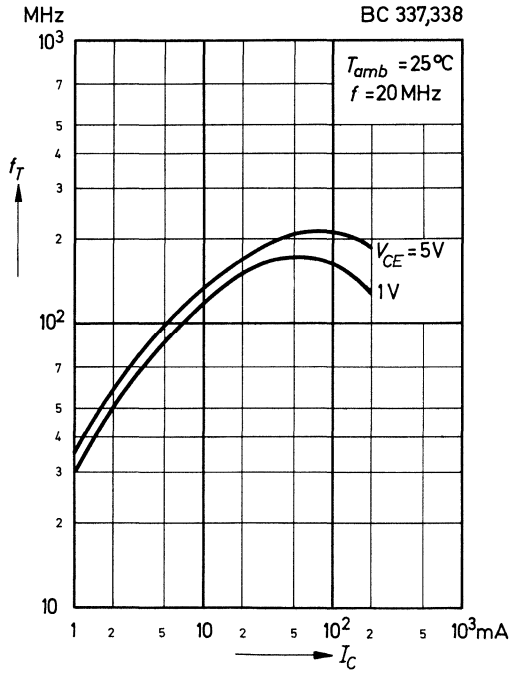


Pulse thermal resistance versus pulse duration

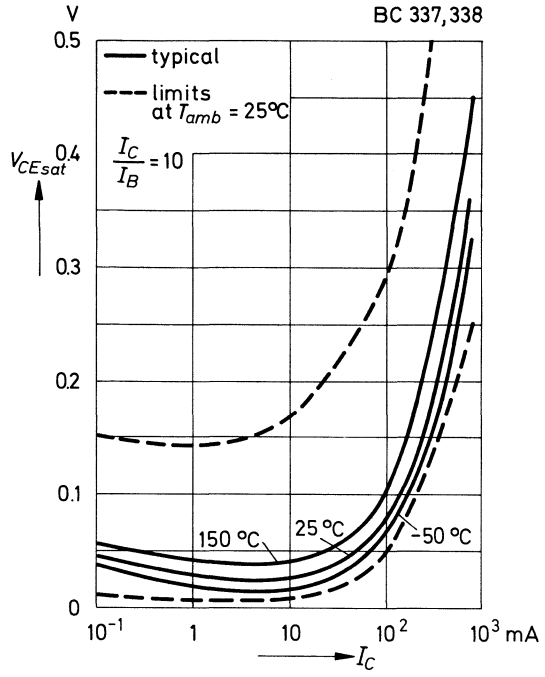
Valid provided that leads are kept at ambient temperature a a distance of 2 mm from case



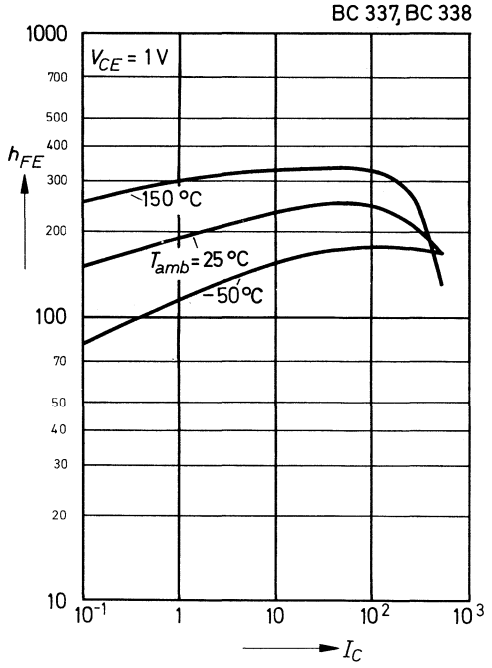
Gain bandwidth product versus collector current



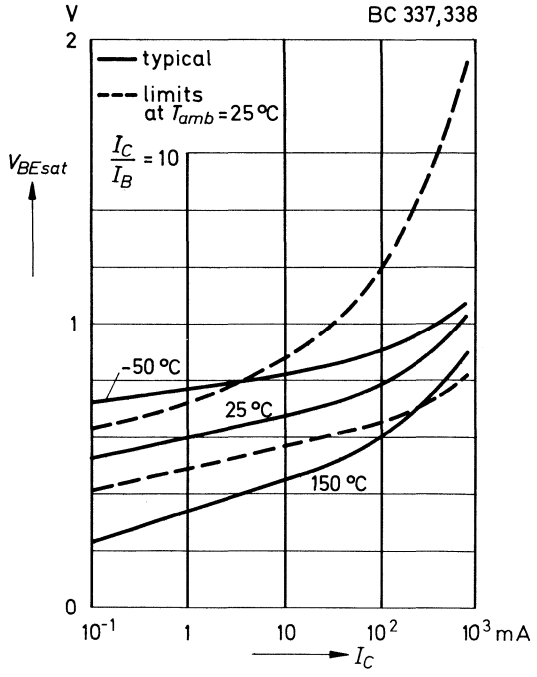
Collector saturation voltage versus collector current



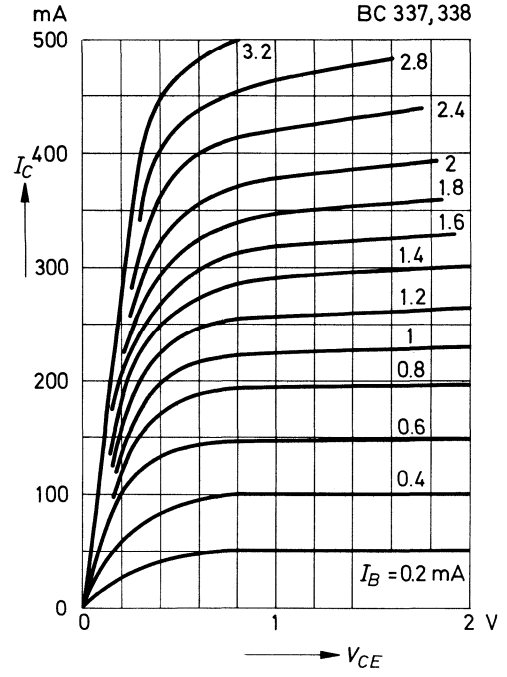
DC current gain versus collector current



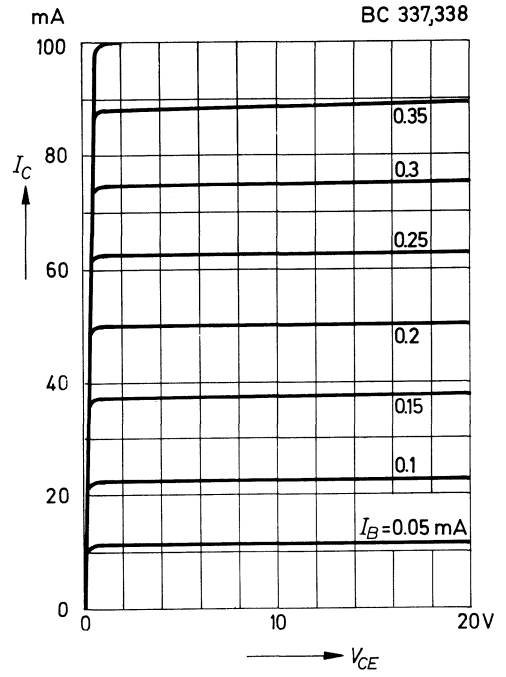
Base saturation voltage versus collector current



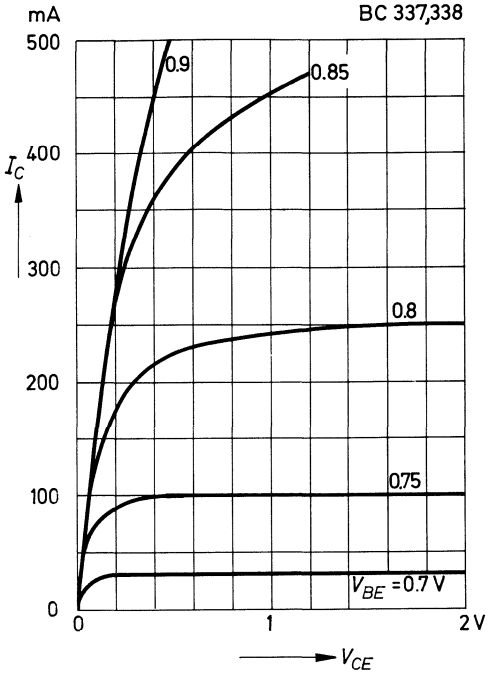
Common emitter collector characteristics



Common emitter collector characteristics



Common emitter collector characteristics

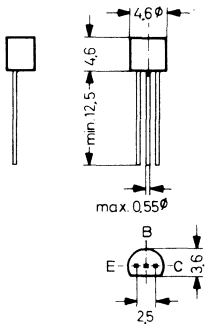


BC413, BC414

NPN Silicon Epitaxial Planar Transistors
for use in high-quality, low-noise AF and DC amplifiers. Complementary types are the PNP transistors BC415 and BC416.

These types are subdivided into two groups B and C according to their current gain.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



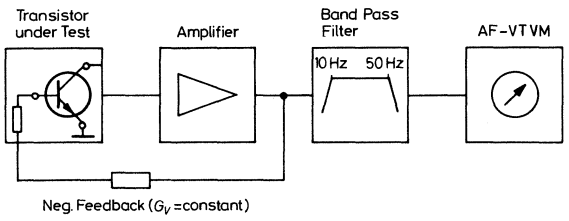
Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC414** **BC413**	V_{CBO} V_{CBO}	50 45	V V
Collector Emitter Voltage	**BC414** **BC413**	V_{CEO} V_{CEO}	45 30	V V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	100	mA
Base Current		I_B	20	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



Test circuit for equivalent noise EMF

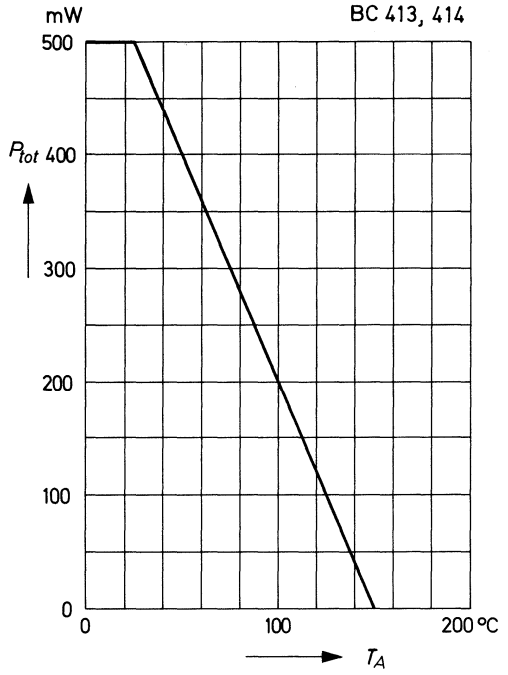
Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz						
Small Signal Current Gain	**Current Gain Group B**	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group B**	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group B**	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio	**Current Gain Group B**	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at V_{CE} = 5 V, I_C = 0.01 mA	**Current Gain Group B**	h_{FE}	100	150	–	–
	C	h_{FE}	100	270	–	–
at V_{CE} =5 V, I_C = 2 mA	**Current Gain Group B**	h_{FE}	180	290	460	–
	C	h_{FE}	380	500	800	–
Thermal Resistance Junction to Ambient		R_{thA}	–	–	250[1]	K/W
Collector Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{CEsat}	–	0.075	0.25	V
at I_C = 100 mA, I_B = 5 mA		V_{CEsat}	–	0.25	0.6	V
Base Saturation Voltage at I_C = 100 mA, I_B = 5 mA		V_{BEsat}	–	0.9	–	V
Base Emitter Voltage						
at V_{CE} = 5 V, I_C = 0.01 mA		V_{BE}	–	0.52	–	V
at V_{CE} = 5 V, I_C = 0.1 mA		V_{BE}	–	0.55	–	V
at V_{CE} = 5 V, I_C = 2 mA		V_{BE}	0.55	0.62	0.75	V
Collector Cutoff Current						
at V_{CB} = 30 V		I_{CBO}	–	–	15	nA
at V_{CB} = 30 V, T_{amb} = 150 °C		I_{CBO}	–	–	5	μA
Emitter Cutoff Current at V_{EB} = 4 V		I_{EBO}	–	–	15	nA
Collector Emitter Breakdown Voltage						
at I_C = 10 mA	**BC414**	$V_{(BR)CEO}$	45	–	–	V
	BC413	$V_{(BR)CEO}$	30	–	–	V
Collector Base Breakdown Voltage						
at I_C = 10 μA	**BC414**	$V_{(BR)CBO}$	50	–	–	V
	BC413	$V_{(BR)CBO}$	45	–	–	V
Emitter Base Breakdown Voltage at I_E = 10 μA		$V_{(BR)EBO}$	5	–	–	V
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		f_T	–	250	–	MHz
Collector Base Capacitance at V_{CBO} = 10 V, f = 1 MHz		C_{CBO}	–	2.5	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 0.2 mA, R_G = 2 kΩ, f = 30 Hz . . . 15 kHz		F	–	–	3	dB
Equivalent Noise EMF (referred to base) at V_{CE} = 5 V, I_C = 0.2 mA, R_G = 2 kΩ, f = 10 . . . 50 Hz		v_r	–	–	0.135	μV

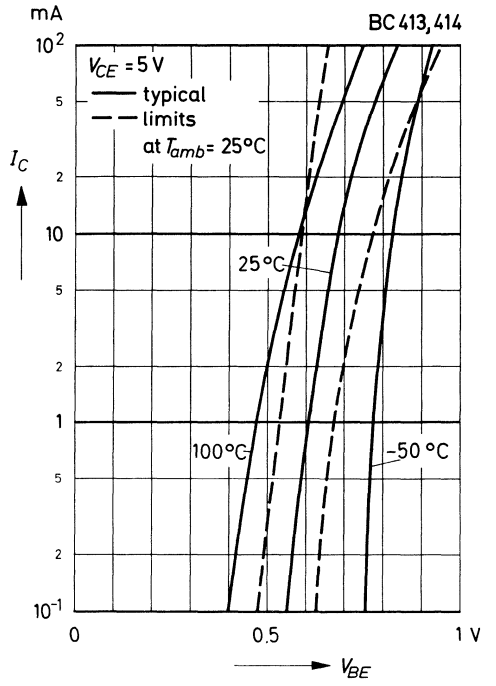
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

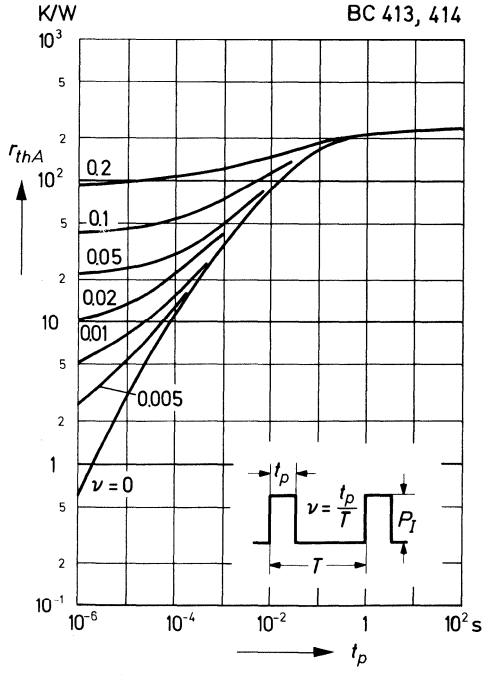


Collector current versus base emitter voltage

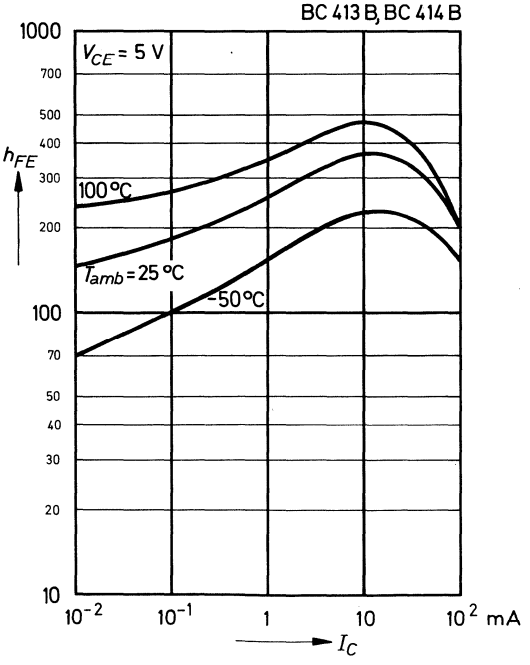


Pulse thermal resistance versus pulse duration

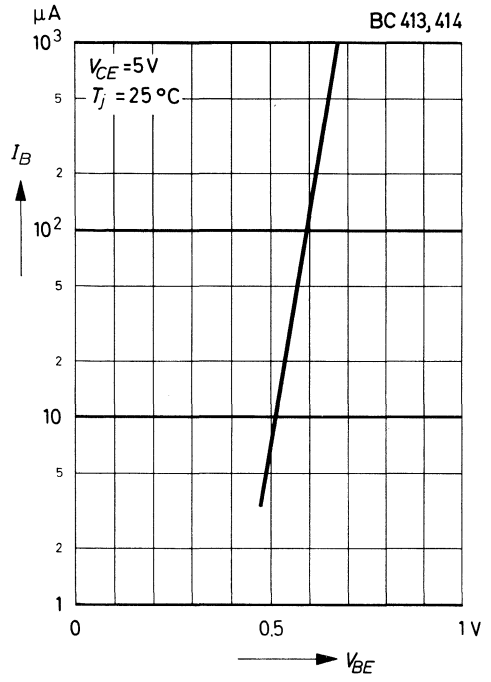
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



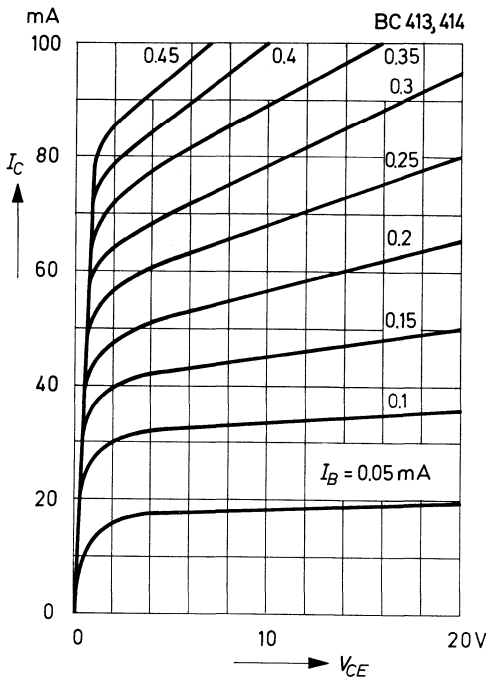
DC current gain versus collector current



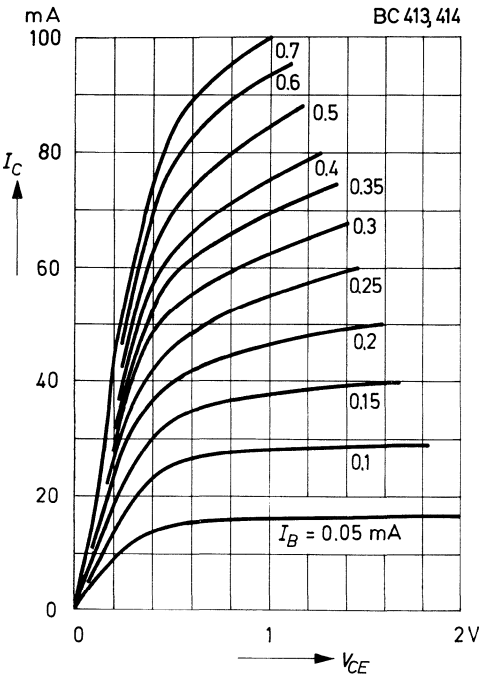
Common emitter input characteristic



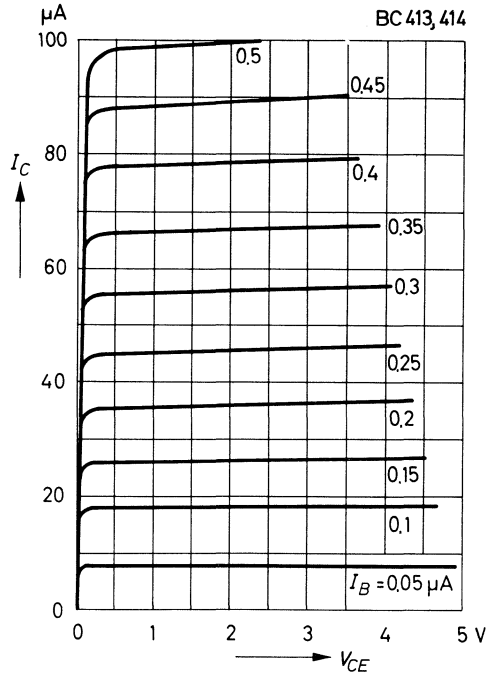
Common emitter collector characteristics



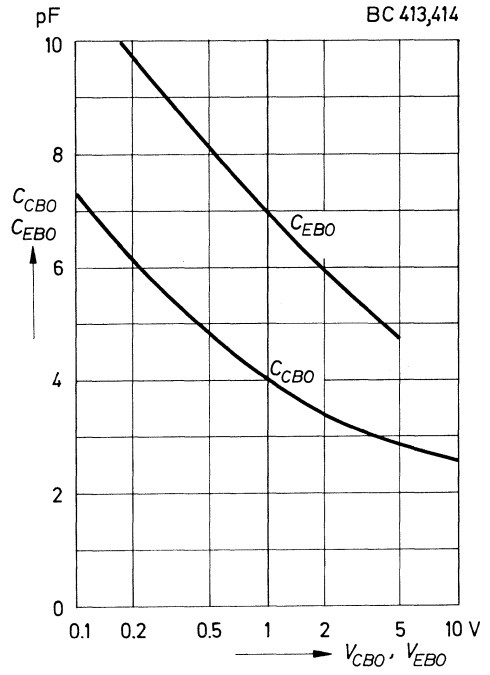
Common emitter collector characteristics



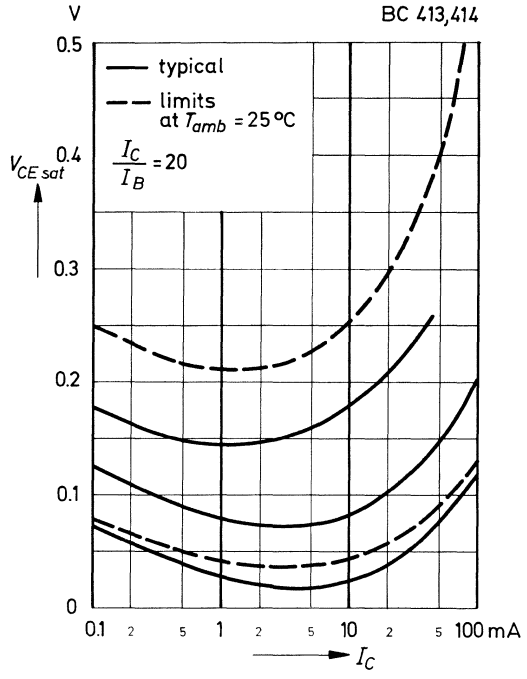
Common emitter input characteristic



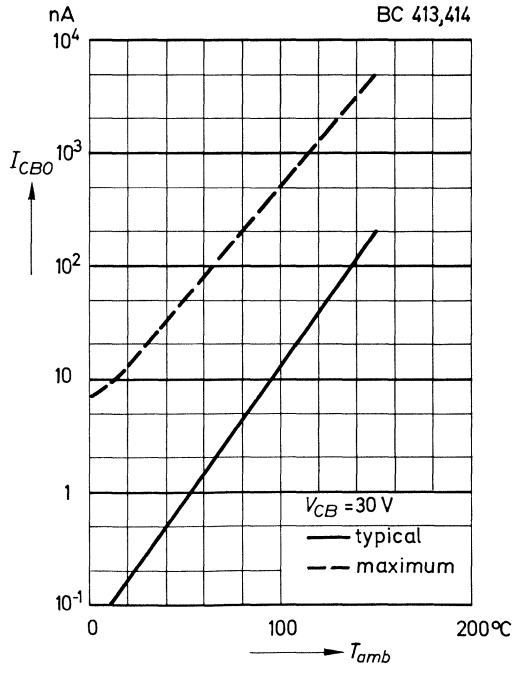
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



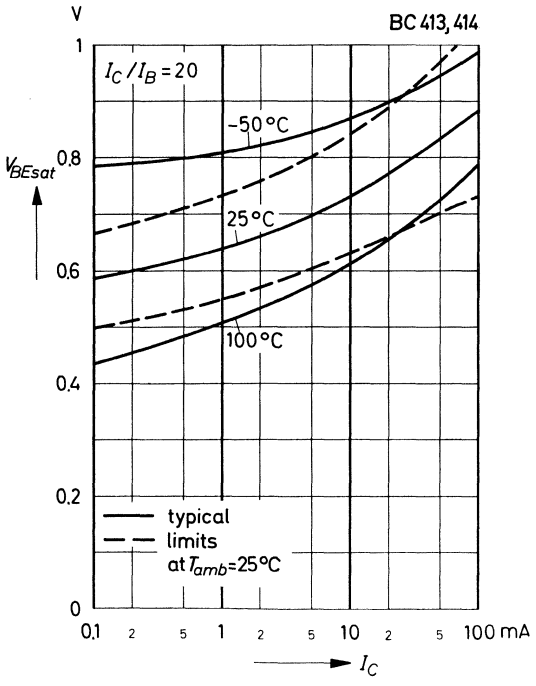
Collector saturation voltage versus collector current



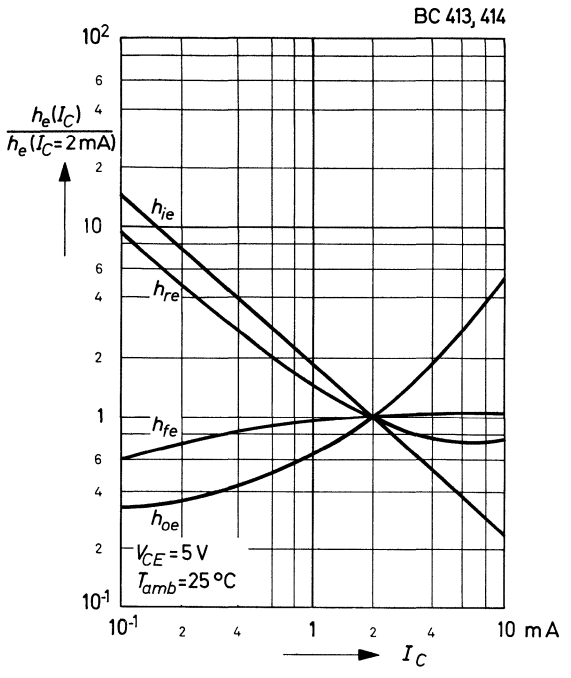
Collector cutoff current versus ambient temperature



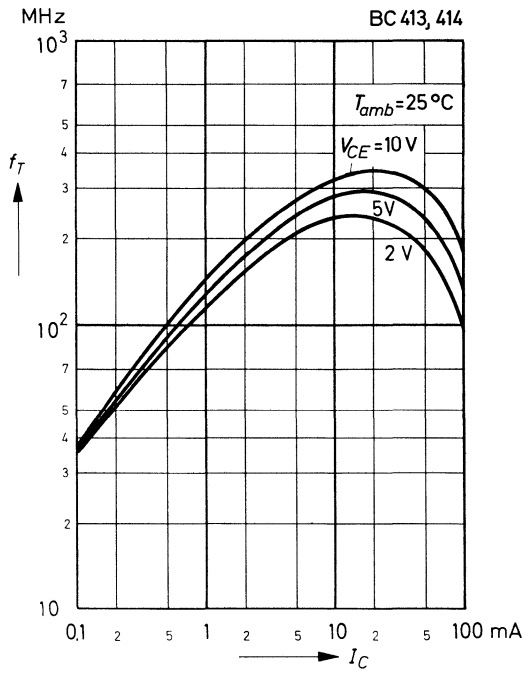
Base saturation voltage versus collector current



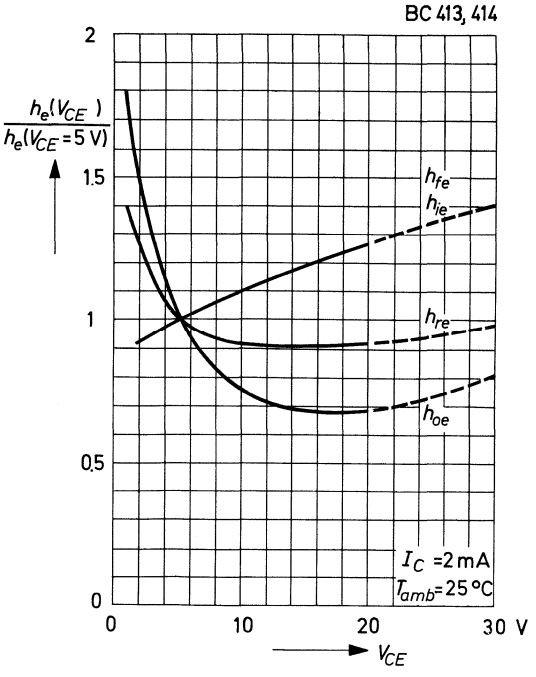
Relative h-parameters versus collector current



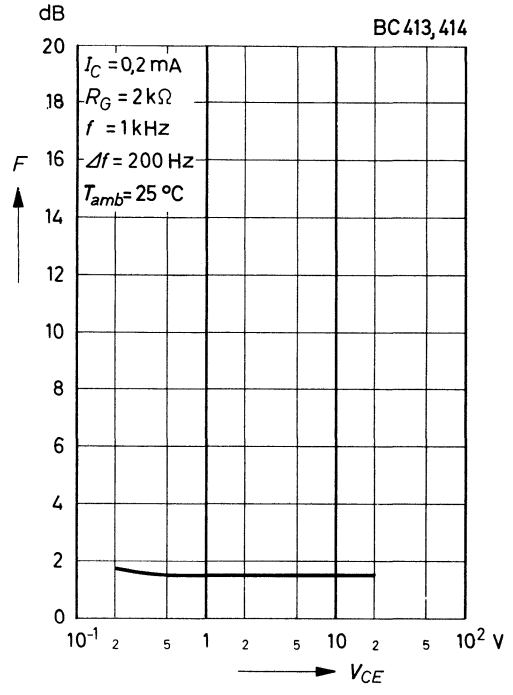
Gain bandwidth product versus collector current



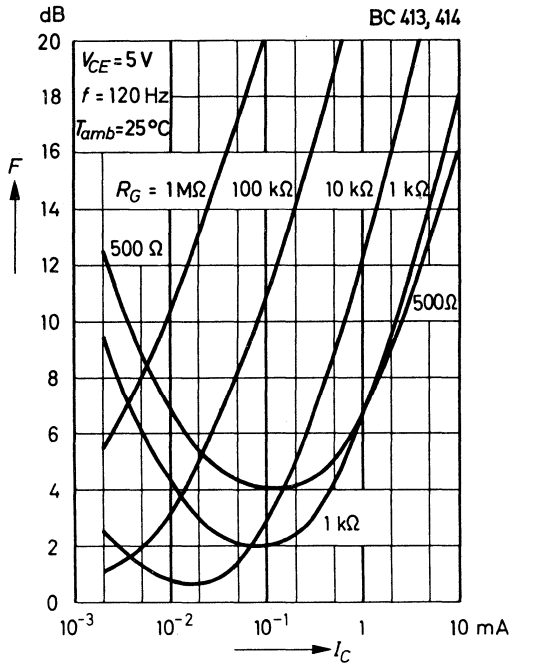
Relative h-parameters versus collector emitter voltage



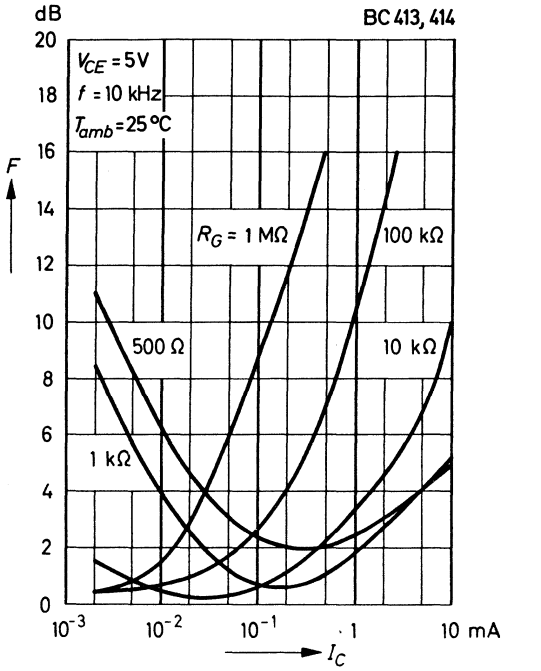
Noise figure versus collector emitter voltage



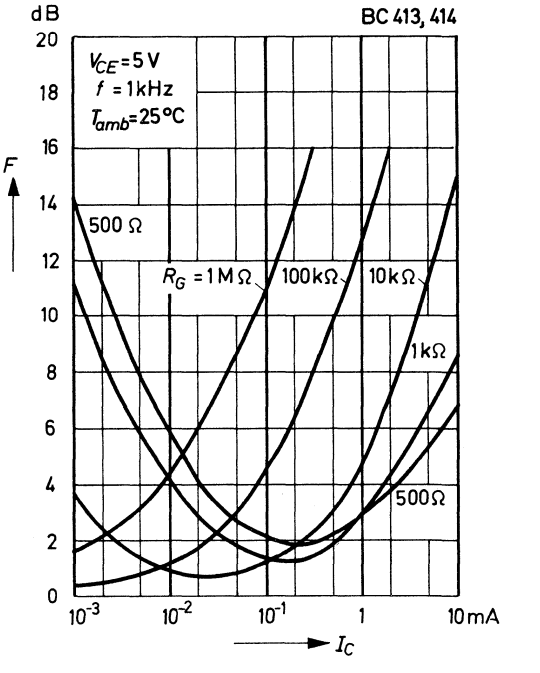
Noise figure versus collector current



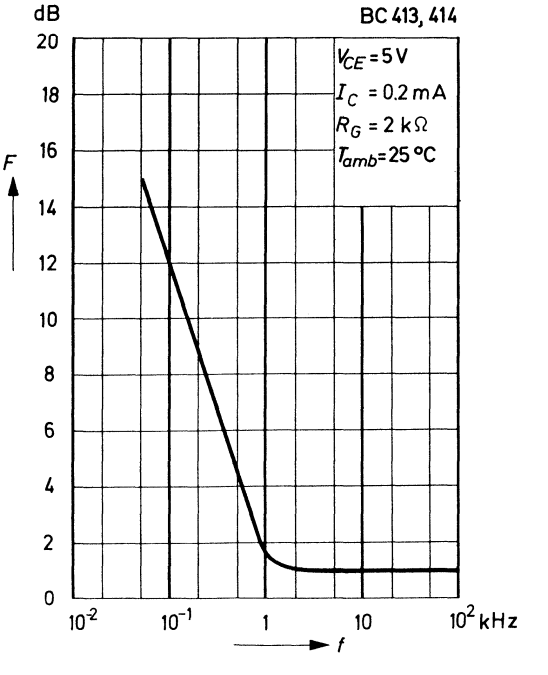
Noise figure versus collector current



Noise figure versus collector current



Noise figure versus frequency

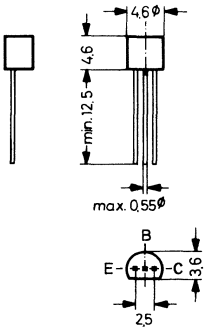


BC445, BC447, BC449

NPN Silicon Epitaxial Planar Transistors
for high voltage drivers and output stages.

As complementary types the PNP transistors BC446, BC448 and BC450 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC445**	V_{CBO}	60	V
	BC447	V_{CBO}	80	V
	BC449	V_{CBO}	100	V
Collector Emitter Voltage	**BC445**	V_{CEO}	60	V
	BC447	V_{CEO}	80	V
	BC449	V_{CEO}	100	V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	300	mA
Power Dissipation at $T_{amb} = 25$ °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 ... +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain						
at V_{CE} = 5 V, I_C = 2 mA		h_{FE}	50	–	460	–
	Current Gain Group A	h_{FE}	120	–	220	–
	Current Gain Group B (only BC445, BC447)	h_{FE}	180	–	460	–
at V_{CE} = 5 V, I_C = 10 mA		h_{FE}	50	–	–	–
	Current Gain Group A	h_{FE}	100	–	–	–
	Current Gain Group B (only BC445, BC447)	h_{FE}	160	–	–	–
at V_{CE} = 5 V, I_C = 100 mA		h_{FE}	50	–	–	–
	Current Gain Group A	h_{FE}	60	–	–	–
	Current Gain Group B (only BC445, BC447)	h_{FE}	90	–	–	–
Thermal Resistance Junction to Ambient		R_{thA}	–	–	200[1]	K/W
Collector Saturation Voltage at I_C = 100 mA, I_B = 10 mA		V_{CEsat}	–	0.1	0.25	V
Base Saturation Voltage at I_C = 100 mA, I_B = 10 mA		V_{BEsat}	–	0.85	–	V
Base Emitter Voltage at V_{CE} = 5 V, I_C = 100 mA		V_{BE}	–	0.8	1.2	V
Collector Emitter Breakdown Voltage						
at I_C = 1 mA	**BC445**	$V_{(BR)CEO}$	60	–	–	V
	BC447	$V_{(BR)CEO}$	80	–	–	V
	BC449	$V_{(BR)CEO}$	100	–	–	V
Collector Base Breakdown Voltage						
at I_C = 100 µA	**BC445**	$V_{(BR)CBO}$	60	–	–	V
	BC447	$V_{(BR)CBO}$	80	–	–	V
	BC449	$V_{(BR)CBO}$	100	–	–	V
Emitter Base Breakdown Voltage at I_E = 10 µA		$V_{(BR)EBO}$	5	–	–	V
Collector Cutoff Current						
at V_{CB} = 30 V	**BC445**	I_{CBO}	–	–	100	nA
at V_{CB} = 40 V	**BC447**	I_{CBO}	–	–	100	nA
at V_{CB} = 60 V	**BC449**	I_{CBO}	–	–	100	nA
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 50 mA, f = 100 MHz		f_T	100	200	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	3	–	pF
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz		C_{EBO}	–	16	–	pF

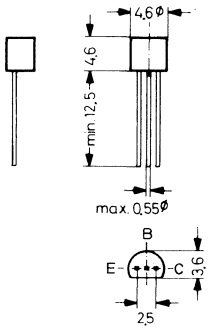
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC546 ... BC550

NPN Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC546 is available in groups A and B, however, the types BC547 and BC548 can be supplied in all three groups. The BC549 and BC550 are low noise types and available in groups B and C. As complementary types the PNP transistors BC556 ... BC560 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC546**	V_{CBO}	80	V
	BC547, BC550	V_{CBO}	50	V
	BC548, BC549	V_{CBO}	30	V
Collector Emitter Voltage	**BC546**	V_{CES}	80	V
	BC547, BC550	V_{CES}	50	V
	BC548, BC549	V_{CES}	30	V
Collector Emitter Voltage	**BC546**	V_{CEO}	65	V
	BC547, BC550	V_{CEO}	45	V
	BC548, BC549	V_{CEO}	30	V
Emitter Base Voltage	**BC546, BC547**	V_{EBO}	6	V
	BC548, BC549	V_{EBO}	5	V
	BC550			
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	200	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 ... +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz						
Small Signal Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio						
	Current Gain Group A	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at V_{CE} = 5 V, I_C = 10μA	**Current Gain Group A**	h_{FE}	–	90	–	–
	B	h_{FE}	–	150	–	–
	C	h_{FE}	–	270	–	–
at V_{CE} = 5 V, I_C = 2 mA	**Current Gain Group A**	h_{FE}	110	180	220	–
	B	h_{FE}	200	290	450	–
	C	h_{FE}	420	500	800	–
at V_{CE} = 5 V, I_C = 100 mA	**Current Gain Group A**	h_{FE}	–	120	–	–
	B	h_{FE}	–	200	–	–
	C	h_{FE}	–	400	–	–
Thermal Resistance Junction to Ambient		R_{thA}	–	–	250[1]	K/W
Collector Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{CEsat}	–	80	200	mV
at I_C = 100 mA, I_B = 5 mA		V_{CEsat}	–	200	600	mV
Base Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{BEsat}	–	700	–	mV
at I_C = 100 mA, I_B = 5 mA		V_{BEsat}	–	900	–	mV
Base Emitter Voltage						
at V_{CE} = 5 V, I_C = 2 mA		V_{BE}	580	660	700	mV
at V_{CE} = 5 V, I_C = 10 mA		V_{BE}	–	–	720	mV
Collector Cutoff Current						
at V_{CE} = 80 V	**BC546**	I_{CES}	–	0.2	15	nA
at V_{CE} = 50 V	**BC547, BC550**	I_{CES}	–	0.2	15	nA
at V_{CE} = 30 V	**BC548, BC549**	I_{CES}	–	0.2	15	nA
at V_{CE} = 80 V, T_j = 125 °C	**BC546**	I_{CES}	–	–	4	μA
at V_{CE} = 50 V, T_j = 125 °C	**BC547, BC550**	I_{CES}	–	–	4	μA
at V_{CE} = 30 V, T_j = 125 °C	**BC548, BC549**	I_{CES}	–	–	4	μA
at V_{CB} = 30 V		I_{CBO}	–	–	15	nA
at V_{CB} = 30 V, T_j = 150 °C		I_{CBO}	–	–	5	μA
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		f_T	–	300	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	3.5	6	pF

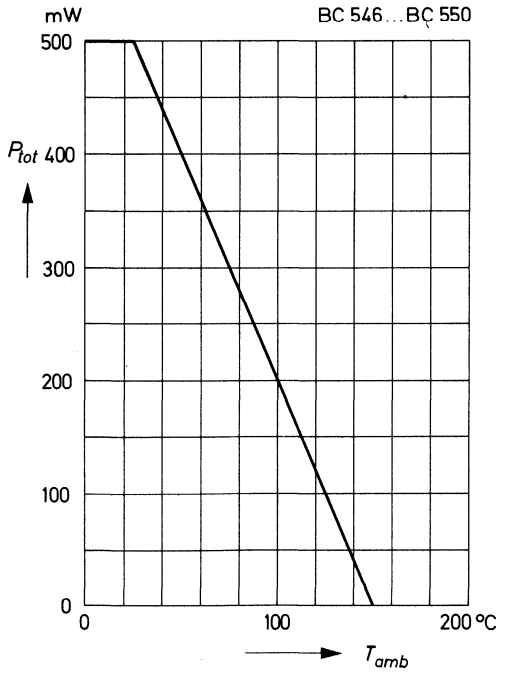
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz	C_{EBO}	–	9	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 1 kHz, $\triangle$f = 200 Hz **BC546, BC547, BC548**	F	–	2	10	dB
BC549, BC550	F	–	1.2	4	dB
at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 30 . . . 15000 Hz **BC549**	F	–	1.4	4	dB
BC550	F	–	1.4	3	dB
Equivalent Noise EMF at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 10 . . . 50 Hz **BC550**	v_r	–	–	0.135	μV

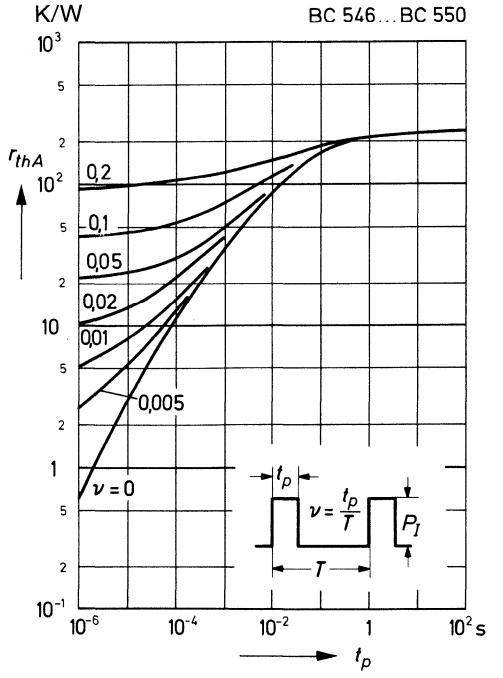
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

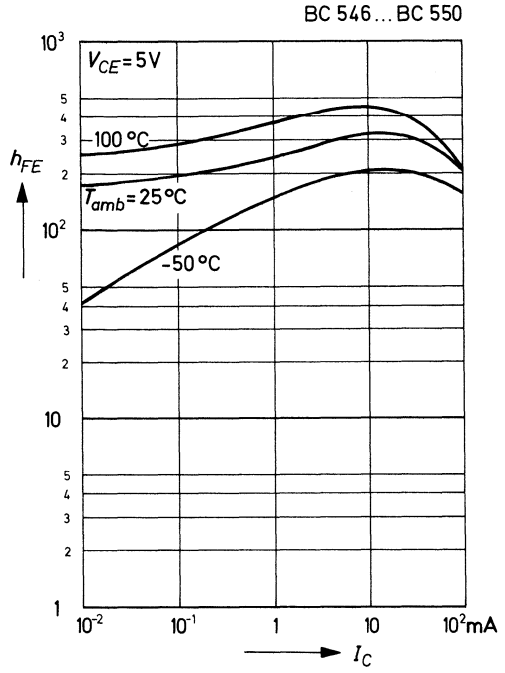


Pulse thermal resistance versus pulse duration

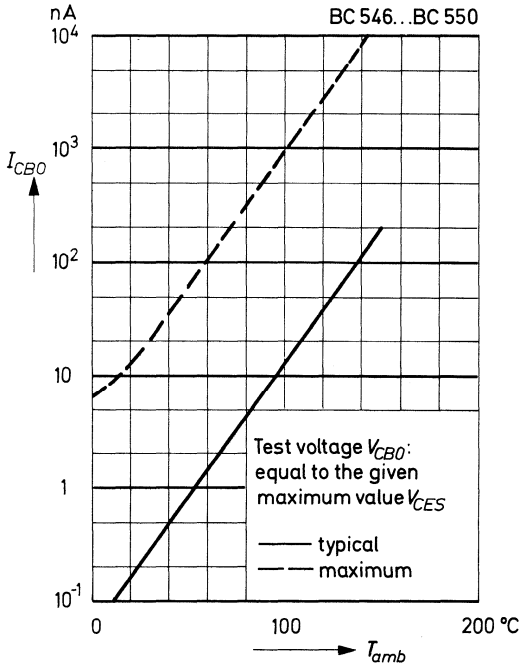
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



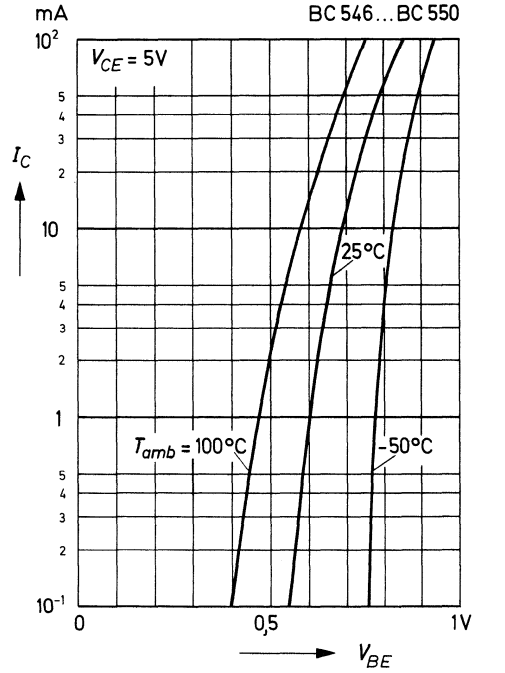
DC current gain versus collector current



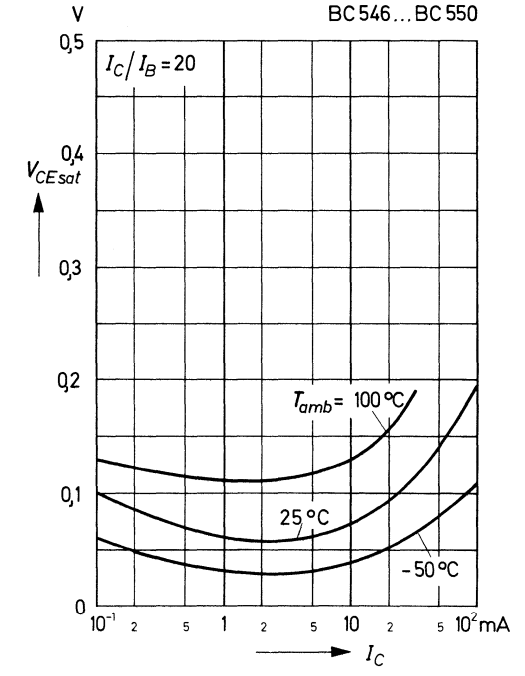
Collector cutoff current versus ambient temperature



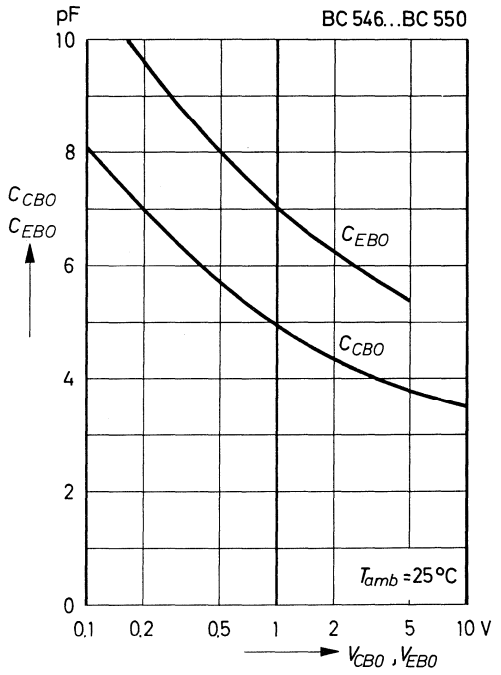
Collector current versus base emitter voltage



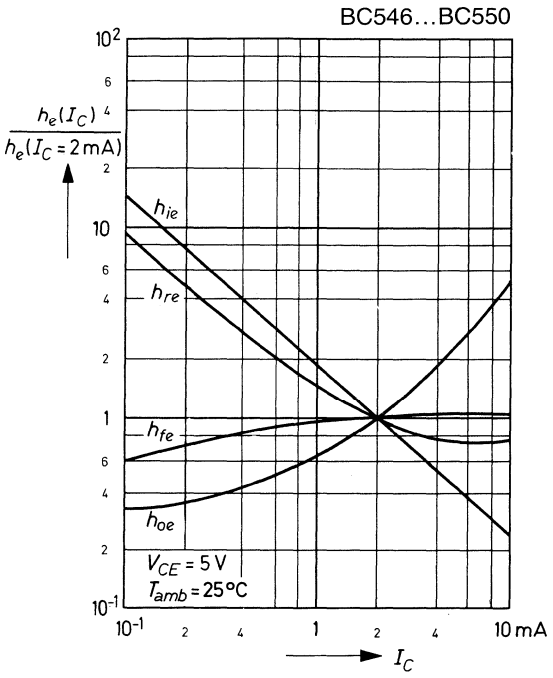
Collector saturation voltage versus collector current



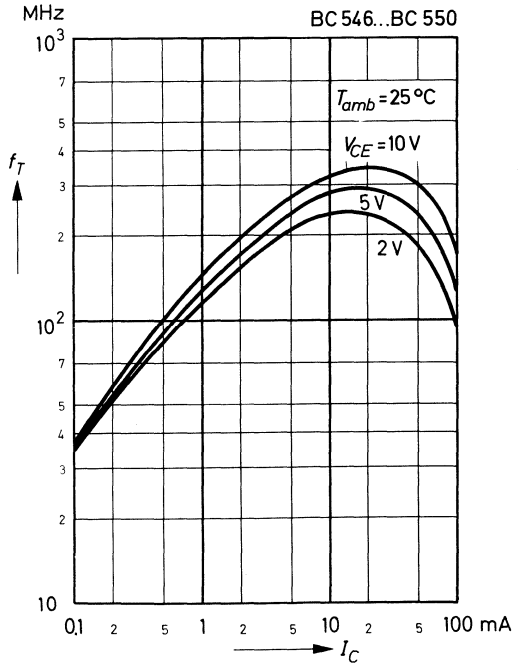
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



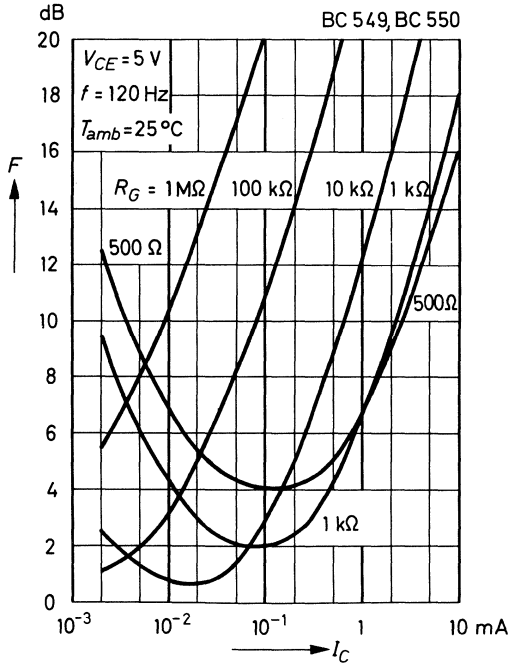
Relative h-parameters versus collector current



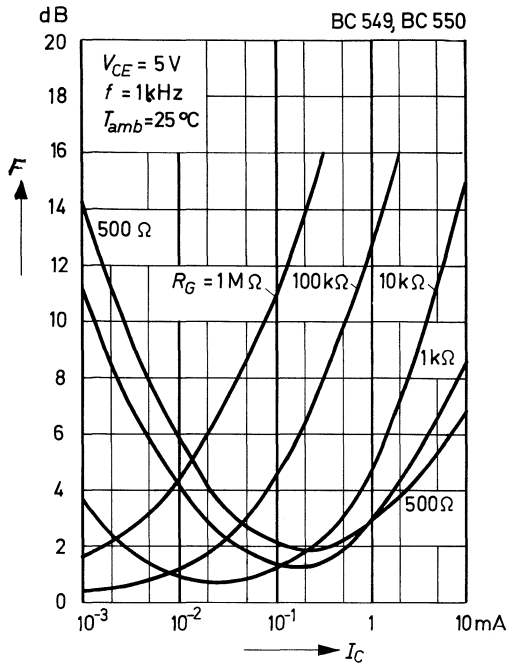
Gain bandwidth product versus collector current



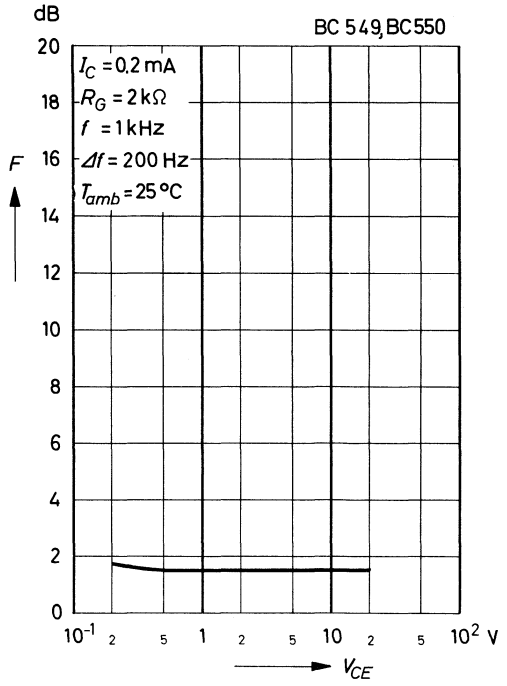
Noise figure versus collector current



Noise figure
versus collector current



Noise figure
versus collector emitter voltage



BC817, BC818

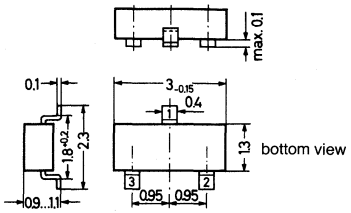
NPN Silicon Epitaxial Planar Transistors
for switching, AF driver and amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups -16, -25 and -40 according to their current gain.
As complementary types the PNP transistors BC807 and BC808 are recommended.
The pinconfiguration of these types is the following:
1 = Collector, 2 = Base, 3 = Emitter.

Marking code

Type	Marking
BC817-16	6A
-25	6B
-40	6C
BC818-16	6E
-25	6F
-40	6G



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC817**	V_{CES}	50	V
	BC818	V_{CES}	30	V
Collector Emitter Voltage	**BC817**	V_{CEO}	45	V
	BC818	V_{CEO}	25	V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	800	mA
Peak Collector Current		I_{CM}	1000	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	1000	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 . . . +150	°C

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

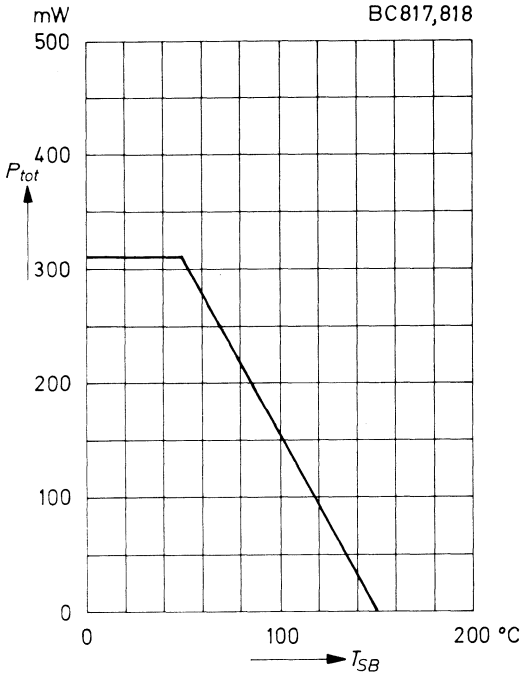
Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain						
at V_{CE} = 1 V, I_C = 100 mA	**Current Gain Group-16**	h_{FE}	100	–	250	–
	-25	h_{FE}	160	–	400	–
	-40	h_{FE}	250	–	600	–
at V_{CE} = 1 V, I_C = 300 mA	**-16**	h_{FE}	60	–	–	–
	-25	h_{FE}	100	–	–	–
	-40	h_{FE}	170	–	–	–
Thermal Resistance Junction Substrate Backside		R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage at I_C = 500 mA, I_B = 50 mA		V_{CEsat}	–	–	0.7	V
Base Emitter Voltage at V_{CE} = 1 V, I_C = 300 mA		V_{BE}	–	–	1.2	V
Collector Cutoff Current						
at V_{CE} = 45 V	**BC817**	I_{CES}	–	–	100	nA
at V_{CE} = 25 V	**BC818**	I_{CES}	–	–	100	nA
at V_{CE} = 25 V, T_j = 150 °C		I_{CES}	–	–	5	μA
Emitter Cutoff Current at V_{EB} = 4 V		I_{EBO}	–	–	100	nA
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz		f_T	–	100	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	12		pF

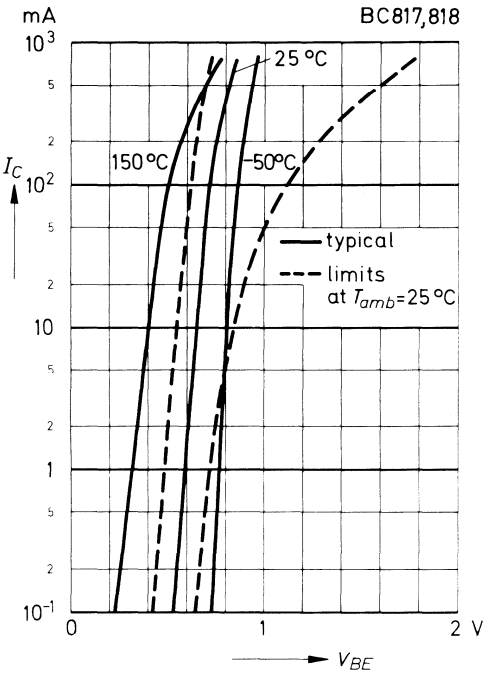
[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Admissible power dissipation versus temperature of substrate backside

Ceramic Substrate 0.7 mm; 2.5 cm² area.

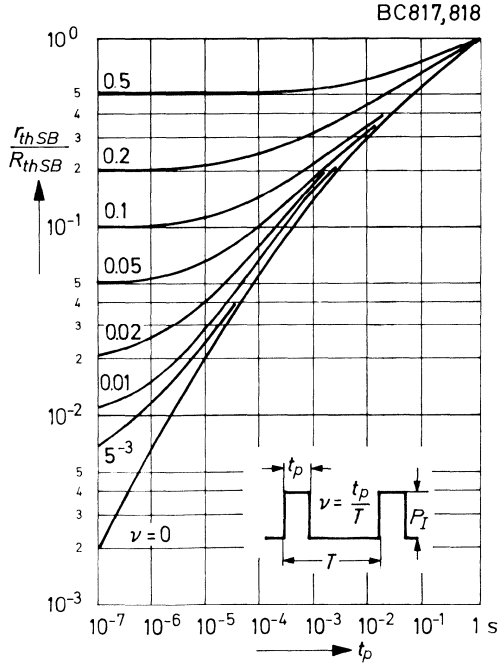


Collector current versus base emitter voltage

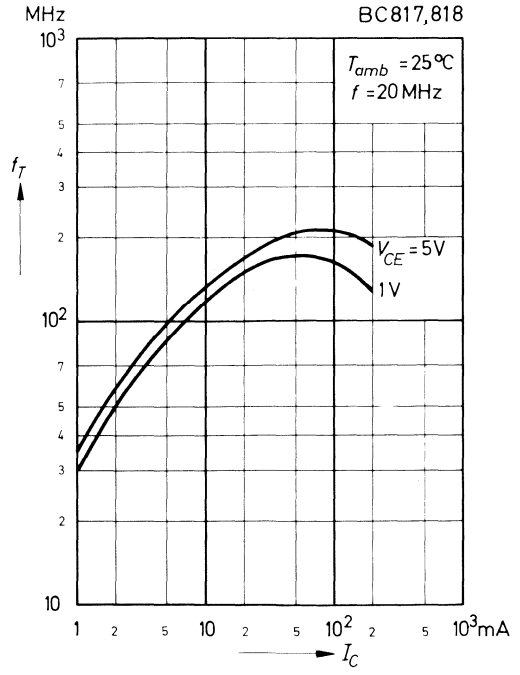


Pulse thermal resistance versus pulse duration (normalized)

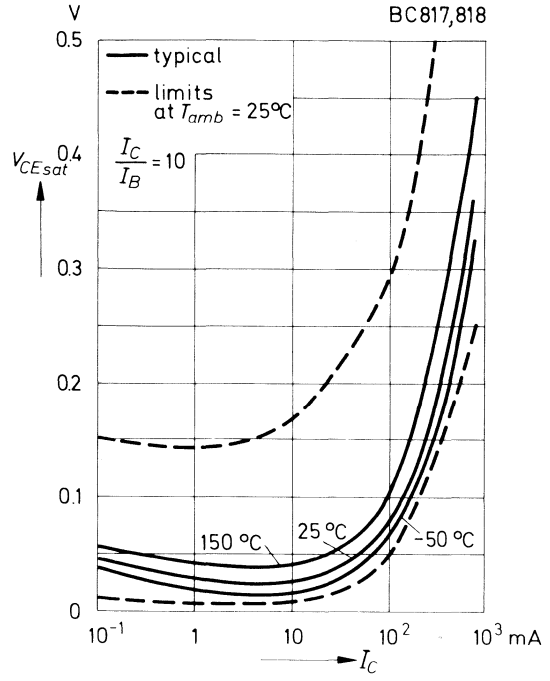
Ceramic Substrate 0.7 mm; 2.5 cm² area.



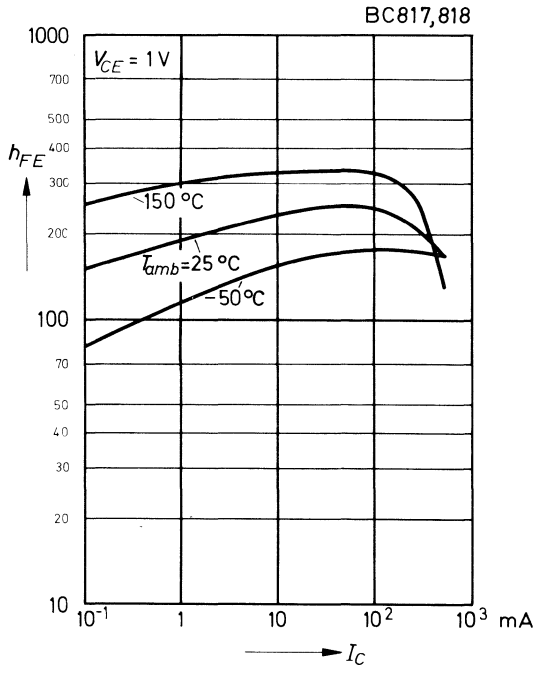
Gain bandwidth product versus collector current



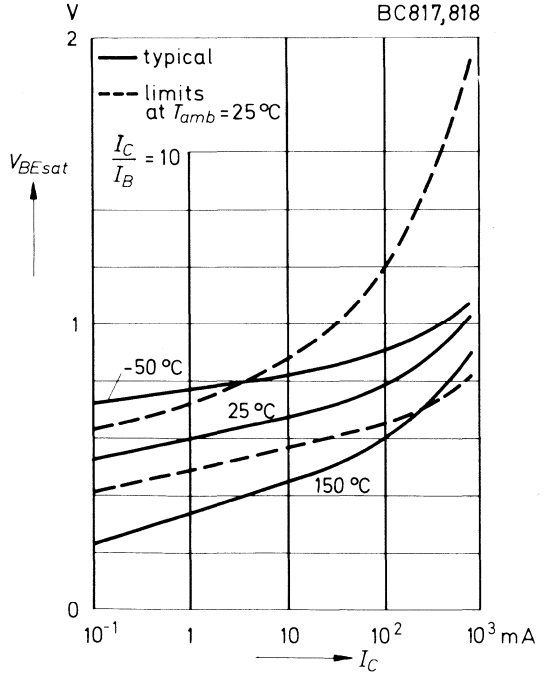
Collector saturation voltage versus collector current



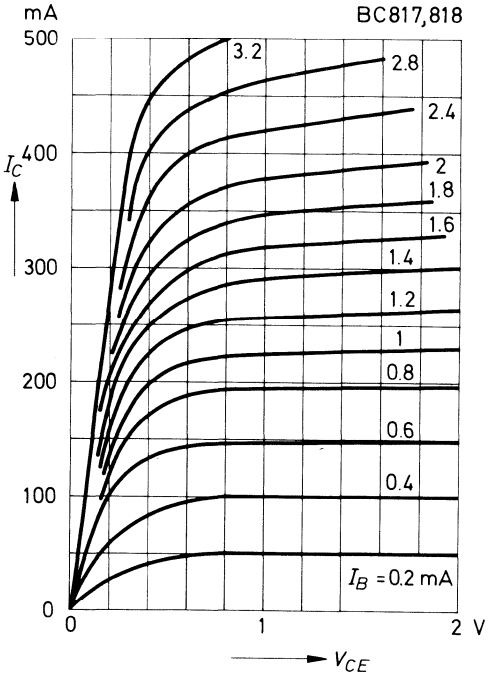
DC current gain versus collector current



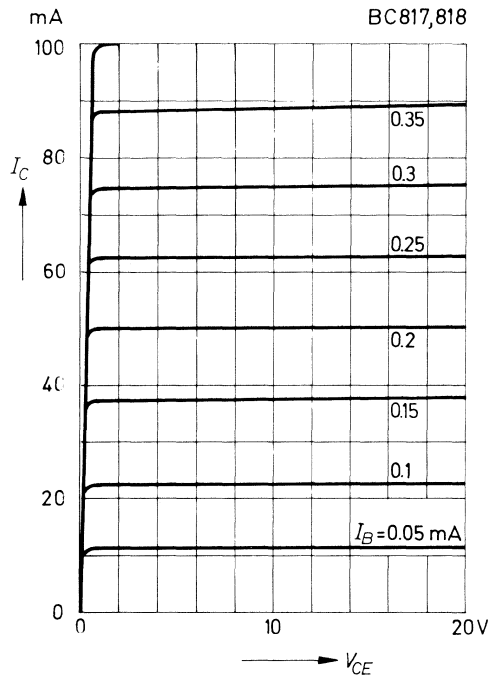
Base saturation voltage versus collector current



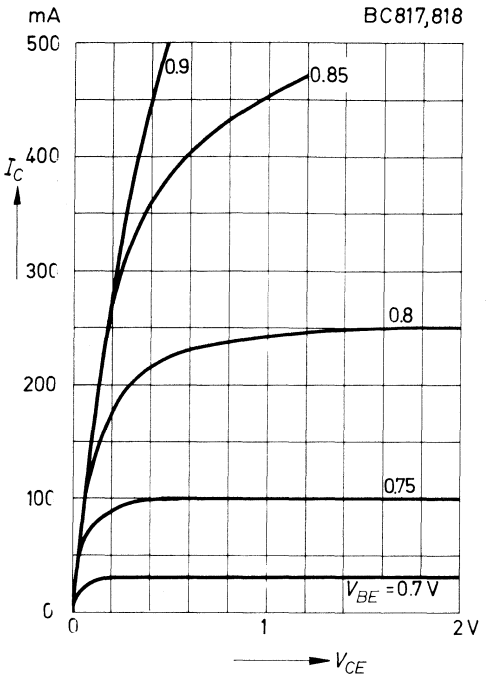
Common emitter collector characteristics



Common emitter collector characteristics



Common emitter collector characteristics

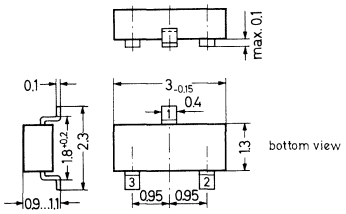


BC846 ... BC850

NPN Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups A, B and C according to their current gain. The types BC846 is available in groups A and B, however, the types BC847 and BC848 can be supplied in all three groups. The BC849 is a low noise type and the BC850 a extremely low noise type. Both are available in groups B and C. As complementary types the PNP transistors BC856...BC860 are recommended.
The pinconfiguration of these types is the following: 1 = Collector, 2 = Base, 3 = Emitter.



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Marking code

Type	Marking
BC846A	1A
B	1B
BC847A	1E
B	1F
C	1G

Marking code

Type	Marking
BC848A	1J
B	1K
C	1L
BC849B	2B
C	2C
BC850B	2F
C	2G

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC846**	V_{CBO}	80	V
	BC847, BC850	V_{CBO}	50	V
	BC848, BC849	V_{CBO}	30	V
Collector Emitter Voltage	**BC846**	V_{CES}	80	V
	BC847, BC850	V_{CES}	50	V
	BC848, BC849	V_{CES}	30	V
Collector Emitter Voltage	**BC846**	V_{CEO}	65	V
	BC847, BC850	V_{CEO}	45	V
	BC848, BC849	V_{CEO}	30	V
Emitter Base Voltage	**BC846, BC847**	V_{EBO}	6	V
	BC848, BC849, BC850	V_{EBO}	5	V
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	200	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 . . . +150	°C

Characteristics at T_{amb} = 25° C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1kHz						
Small Signal Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8,5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio						
	Current Gain Group A	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at V_{CE} = 5 V, I_C = 10 μA	**Current Gain Group A**	h_{FE}	–	90	–	–
	B	h_{FE}	–	150	–	–
	C	h_{FE}	–	270	–	–
at V_{CE} = 5 V, I_C = 2 mA	**Current Gain Group A**	h_{FE}	110	180	220	–
	B	h_{FE}	200	290	450	–
	C	h_{FE}	420	520	800	–
Thermal Resistance Junction to Substrate Backside		R_{thSB}	–	–	320[1]	K/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage						
at I_C = 10 mA, I_B = 0,5 mA		V_{CEsat}	–	90	250	mV
at I_C = 100 mA, I_B = 5 mA		V_{CEsat}	–	200	600	mV
Base Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{BEsat}	–	700	–	mV
at I_C = 100 mA, I_B = 5 mA		V_{BEsat}	–	900	–	mV
Base Emitter Voltage						
at V_{CE} = 5 V, I_C = 2 mA		V_{BE}	580	660	700	mV
at V_{CE} = 5 V, I_C = 10 mA		V_{BE}	–	–	720	mV
Collector Cutoff Current						
at V_{CE} = 80 V	**BC846**	I_{CES}	–	0.2	15	nA
at V_{CE} = 50 V	**BC847, BC850**	I_{CES}	–	0.2	15	nA
at V_{CE} = 30 V	**BC848, BC849**	I_{CES}	–	0.2	15	nA
at V_{CE} = 80 V, T_j = 125 °C	**BC846**	I_{CES}	–	–	4	μA
at V_{CE} = 50 V, T_j = 125 °C	**BC847, BC850**	I_{CES}	–	–	4	μA
at V_{CE} = 30 V, T_j = 125 °C	**BC848, BC849**	I_{CES}	–	–	4	μA
at V_{CB} = 30 V		I_{CBO}	–	–	15	nA
at V_{CB} = 30 V, T_j = 150 °C		I_{CBO}	–	–	5	μA
Gain Bandwidth Product						
at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		f_T	–	300	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	3.5	6	pF
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz		C_{EBO}	–	9	–	pF
Noise Figure						
at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ						
f = 1 kHz, △f = 200 Hz	**BC846, BC847, BC848**	F	–	2	10	dB
	BC849, BC850	F	–	1.2	4	dB
at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ,						
f = 30 ... 15000 Hz	**BC849**	F	–	1.4	4	dB
	BC850	F	–	1.4	3	dB

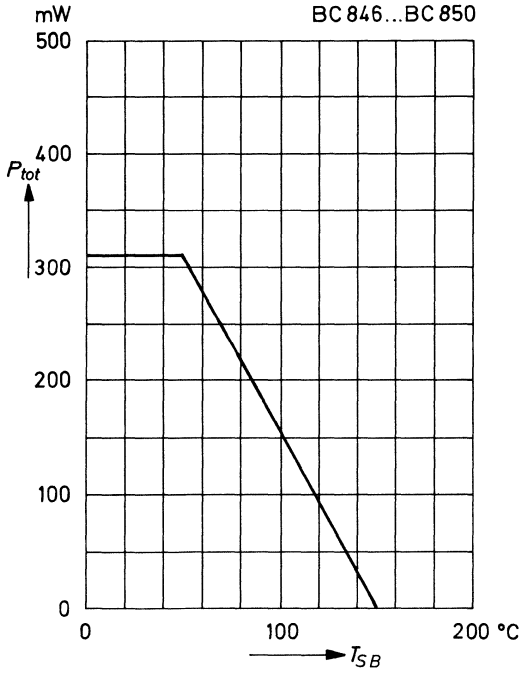
[1] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Equivalent Noise EMF at $V_{CE} = 5$ V, $I_C = 200\ \mu$A, $R_G = 2\ k\Omega$, f = 10 . . . 50 Hz **BC850**	v_r	–	–	0.135	μV

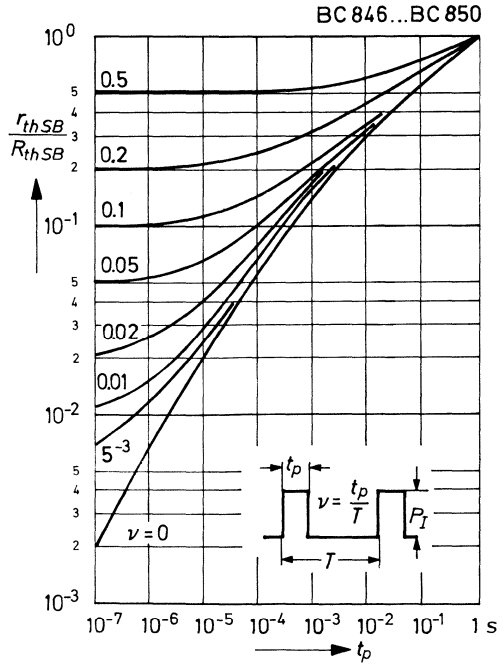
Admissible power dissipation versus temperature of substrate backside

Ceramic Substrate 0.7 mm; 2.5 cm² area.

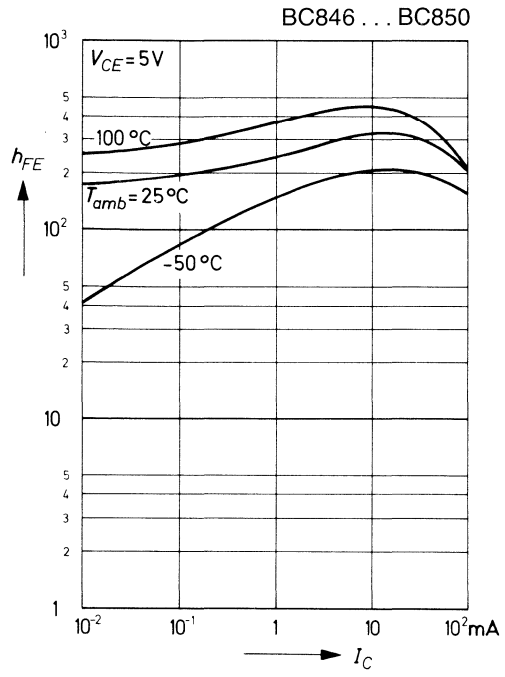


Pulse thermal resistance versus pulse duration (normalized)

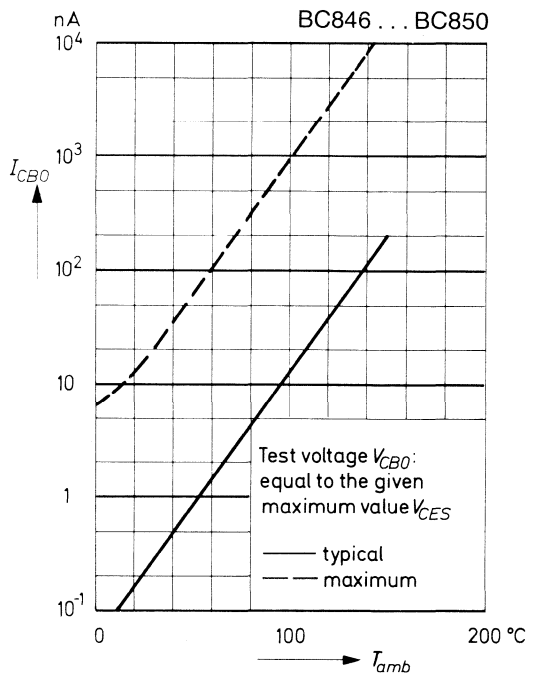
Ceramic Substrate 0.7 mm; 2.5 cm² area.



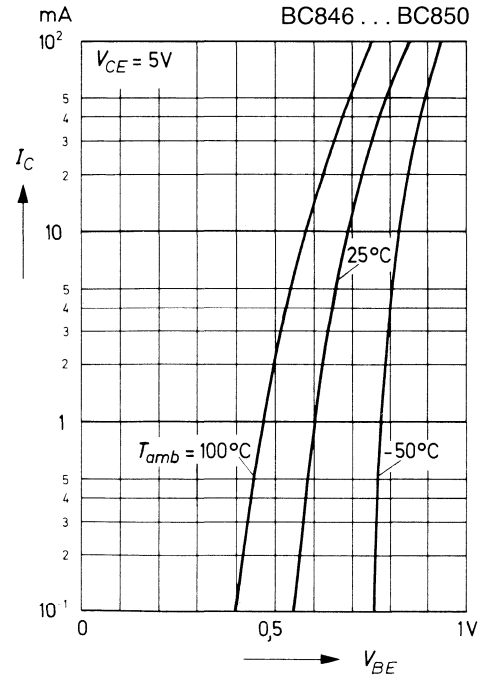
DC current gain versus collector current



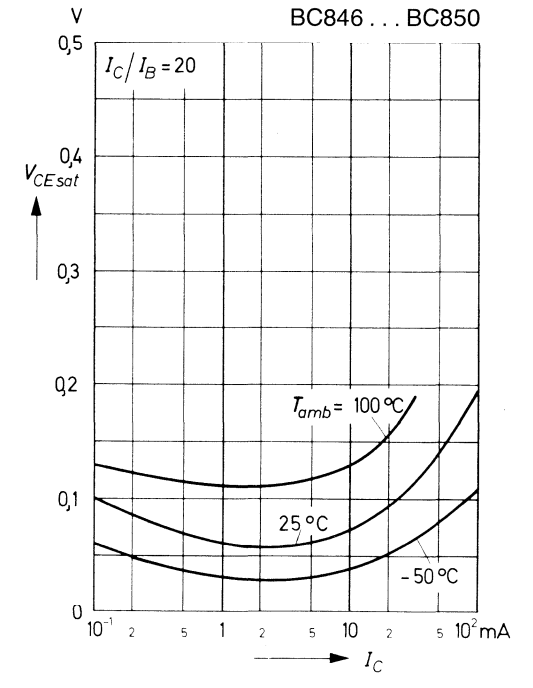
Collector cutoff current versus ambient temperature



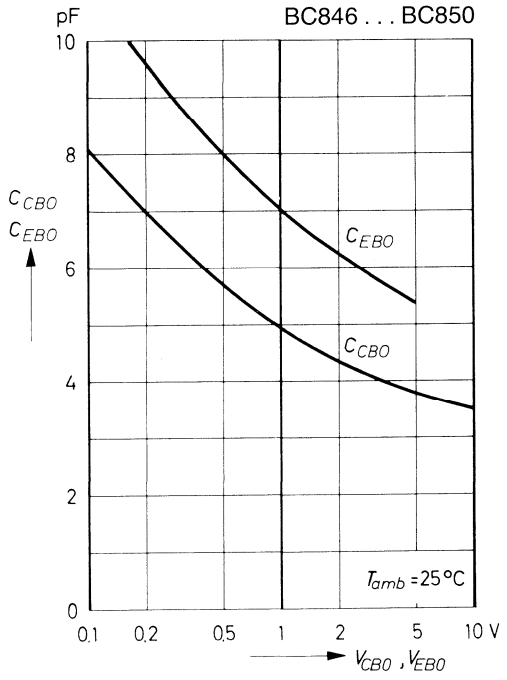
Collector current versus base emitter voltage



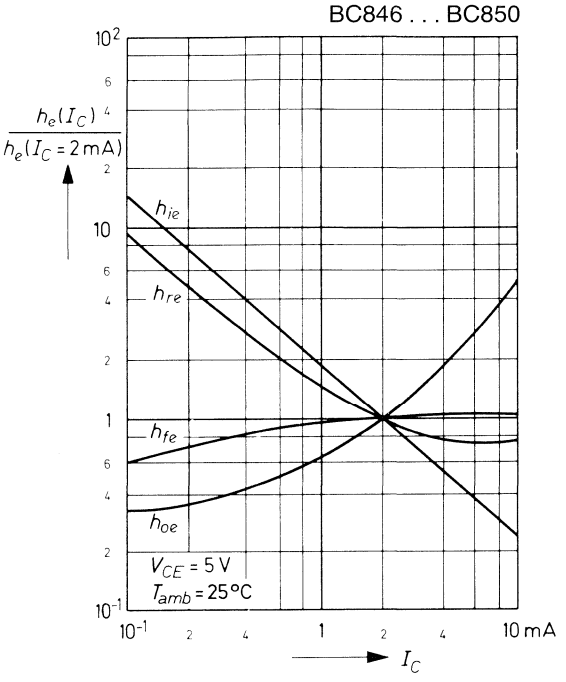
Collector saturation voltage versus collector current



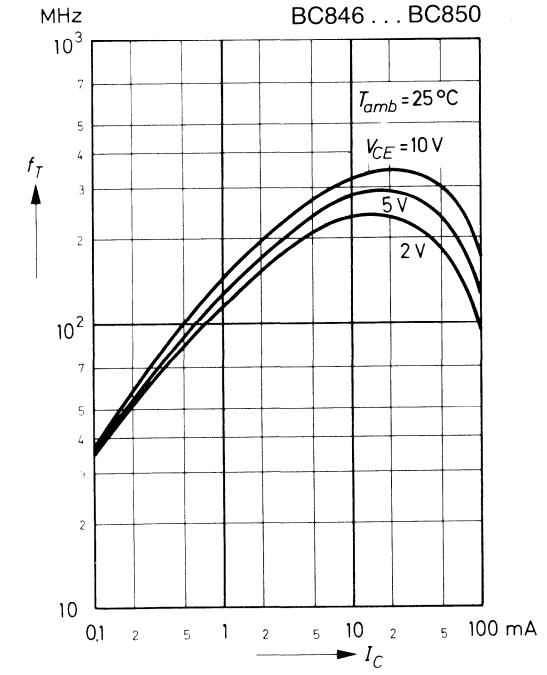
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



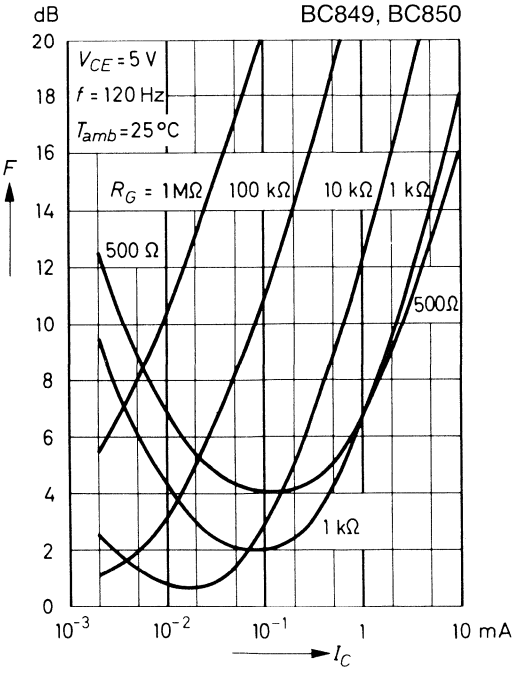
Relative h-parameters versus collector current



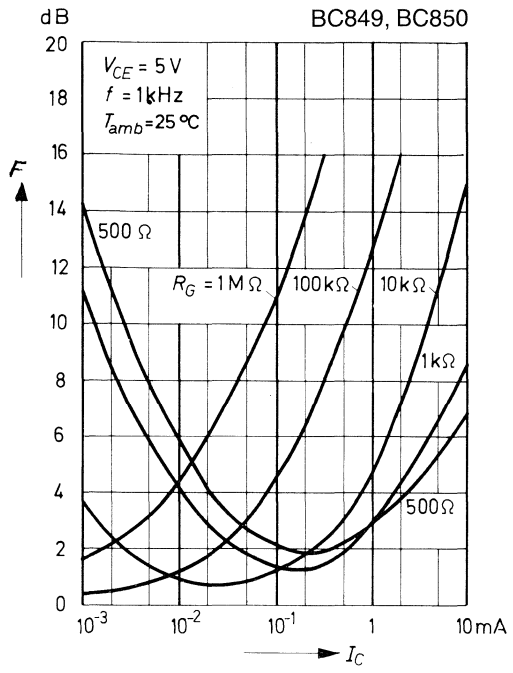
Gain bandwidth product versus collector current



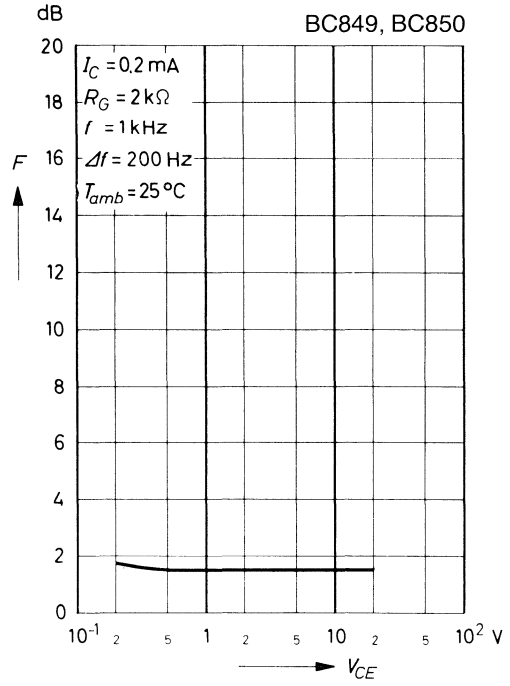
Noise figure versus collector current



Noise figure
versus collector current



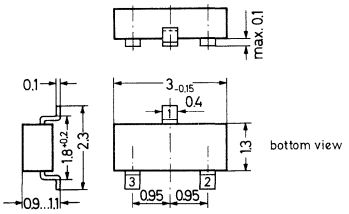
Noise figure
versus collector emitter voltage



BCW60, BCX70

NPN Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.
These transistors BCW60 are subdivided into the groups A, B, C and D, the transistors BCX70 into the groups G, H, J and K according to their current gain. As complementary types the PNP transistors BCW61 and BCX71 are recommended.
The pinconfiguration of these types is the following: 1 = Collector, 2 = Base, 3 = Emitter.



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Marking code

Type	Marking
BCW60A	AA
BCW60B	AB
BCW60C	AC
BCW60D	AD

Marking code

Type	Marking
BCX70G	AG
BCX70H	AH
BCX70J	AJ
BCX70K	AK

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BCW60**	V_{CES}	32	V
	BCX70	V_{CES}	45	V
Collector Emitter Voltage	**BCW60**	V_{CEO}	32	V
	BCX70	V_{CEO}	45	V
Emitter Base Voltage		V_{EBO}	5	V
Collector Current		I_C	200	mA
Base Current		I_B	50	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 to +150	°C

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz						
Small Signal Current Gain	**Group A, G**	h_{fe}	–	200	–	–
	B, H	h_{fe}	–	260	–	–
	C, J	h_{fe}	–	330	–	–
	D, K	h_{fe}	–	520	–	–
Input Impedance	**Group A, G**	h_{ie}	1.6	2.7	4.5	kΩ
	B, H	h_{ie}	2.5	3.6	6	kΩ
	C, J	h_{ie}	3.2	4.5	8.5	kΩ
	D, K	h_{ie}	4.5	7.5	12	kΩ
Output Admittance	**Group A, G**	h_{oe}	–	18	30	μS
	B, H	h_{oe}	–	24	50	μS
	C, J	h_{oe}	–	30	60	μS
	D, K	h_{oe}	–	50	100	μS
Reverse Voltage Transfer Ratio	**Group A, G**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B, H	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C, J	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	D, K	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at V_{CE} = 5 V, I_C = 10 μA	**Group A, G**	h_{FE}	–	78	–	–
	B, H	h_{FE}	20	145	–	–
	C, J	h_{FE}	40	220	–	–
	D, K	h_{FE}	100	300	–	–
at V_{CE} = 5 V, I_C = 2 mA	**Group A, G**	h_{FE}	120	170	220	–
	B, H	h_{FE}	180	250	310	–
	C, J	h_{FE}	250	350	460	–
	D, K	h_{FE}	380	500	630	–
at V_{CE} = 1 V, I_C = 50 mA	**Group A, G**	h_{FE}	50	–	–	–
	B, H	h_{FE}	70	–	–	–
	C, J	h_{FE}	90	–	–	–
	D, K	h_{FE}	100	–	–	–
Thermal Resistance Junction to Substrate Backside		R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage						
at I_C = 10 mA, I_B = 0.25 mA		V_{CEsat}	–	120	350	mV
at I_C = 50 mA, I_B = 1.25 mA		V_{CEsat}	–	200	550	mV
Base Saturation Voltage						
at I_C = 10 mA, I_B = 0.25 mA		V_{BEsat}	–	700	850	mV
at I_C = 50 mA, I_B = 1.25 mA		V_{BEsat}	–	830	1050	mV
Base Emitter Voltage						
at V_{CE} = 5 V, I_C = 10 μA		V_{BE}	–	520	–	mV
at V_{CE} = 5 V, I_C = 2 mA		V_{BE}	550	650	750	mV
at V_{CE} = 1 V, I_C = 50 mA		V_{BE}	–	780	–	mV
Collector Cutoff Current						
at V_{CE} = 32 V	**BCW60**	I_{CES}	–	–	20	nA
at V_{CE} = 32 V, T_{amb} = 150 °C		I_{CES}	–	–	20	μA
at V_{CE} = 45 V	**BCX70**	I_{CES}	–	–	20	nA
at V_{CE} = 45 V, T_{amb} = 150 °C		I_{CES}	–	–	20	μA
Emitter Cutoff Current		I_{EBO}	–	–	20	nA
at V_{EB} = 4 V						
Collector Emitter Breakdown Voltage						
at I_C = 2 mA	**BCW60**	$V_{(BR)CEO}$	32	–	–	V
	BCX70	$V_{(BR)CEO}$	45	–	–	V

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Emitter Base Breakdown Voltage at I_E = 1 μA	$V_{(BR)EBO}$	5	–	–	V
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz	f_T	125	250	–	MHz
Collector Base Capacitance at V_{CEB} = 10 V, f = 1 MHz	C_{CBO}	–	–	4.5	pF
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz	C_{EBO}	–	8	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 1 kHz, $\triangle$f = 200 Hz	F	–	2	6	dB
Switching Times (see Fig. 1) at I_C = 10 mA, I_{B1} = $-I_{B2}$ = 1 mA, R_1 = 5 kΩ, R_2 = 5 kΩ, $-V_{BB}$ = 3.6 V, R_L = 990 kΩ					
Delay Time	t_d	–	35	–	ns
Rise Time	t_r	–	50	–	ns
Turn-On Time	$t_d + t_r$	–	85	150	ns
Storage Time	t_s	–	400	–	ns
Fall Time	t_f	–	80	–	ns
Turn-Off Time	$t_s + t_f$	–	480	800	ns

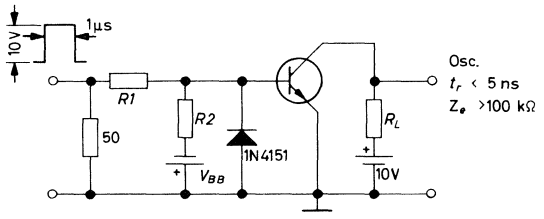
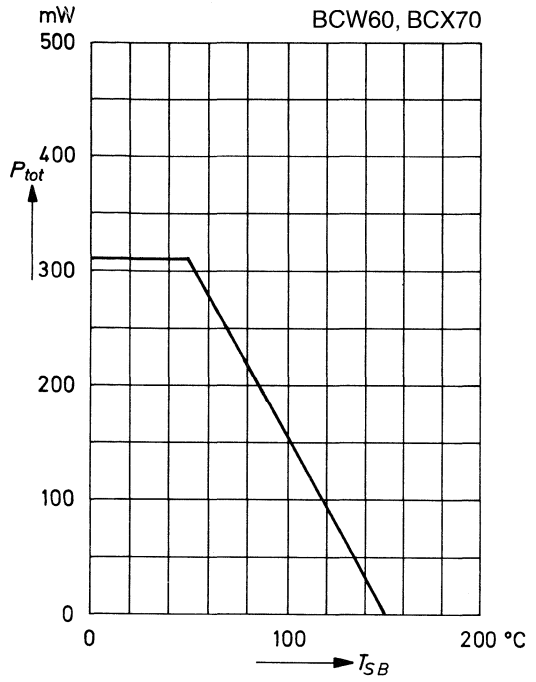


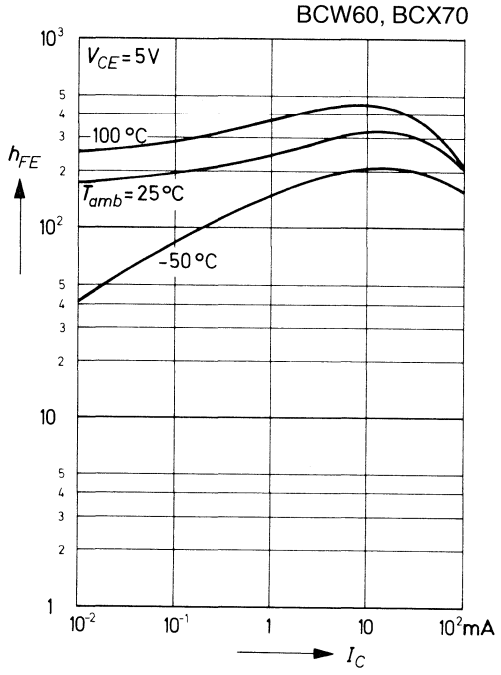
Fig. 1:
Test circuit for switching times

Admissible power dissipation versus temperature of substrate backside

Ceramic Substrate 0.7 mm; 2.5 cm² area.

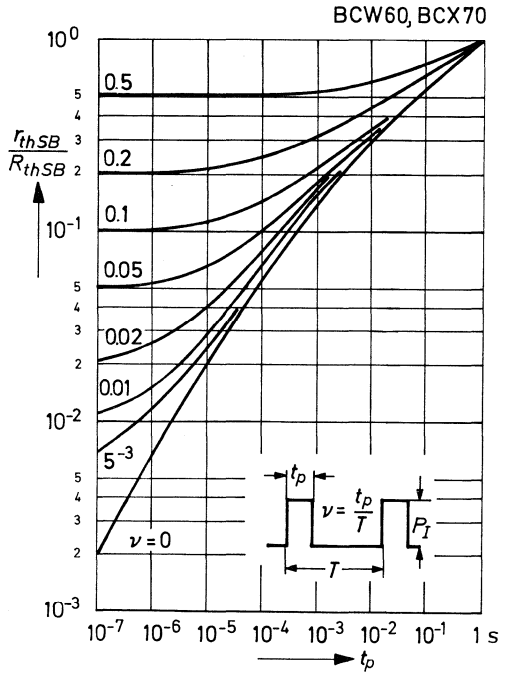


DC current gain versus collector current

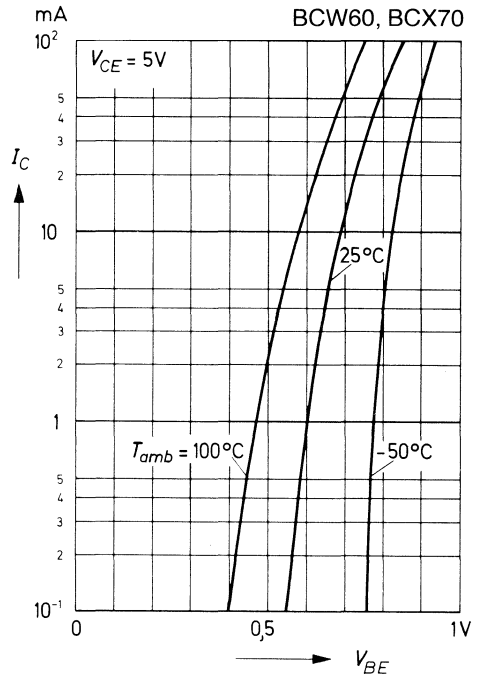


Pulse thermal resistance versus pulse duration (normalized)

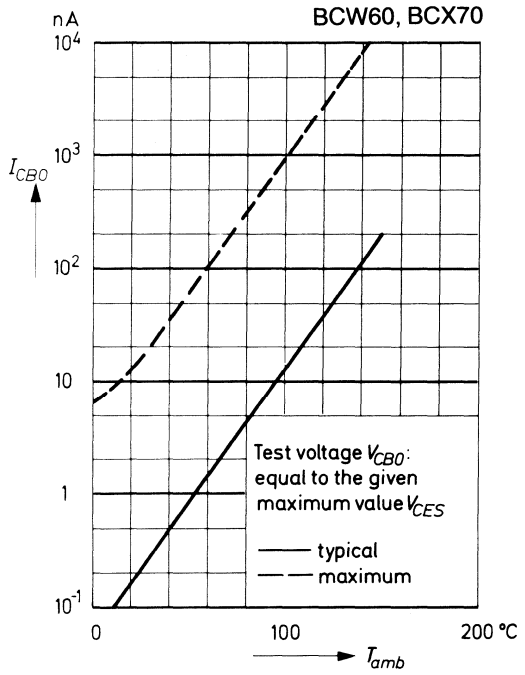
Ceramic Substrate 0.7 mm; 2.5 cm² area.



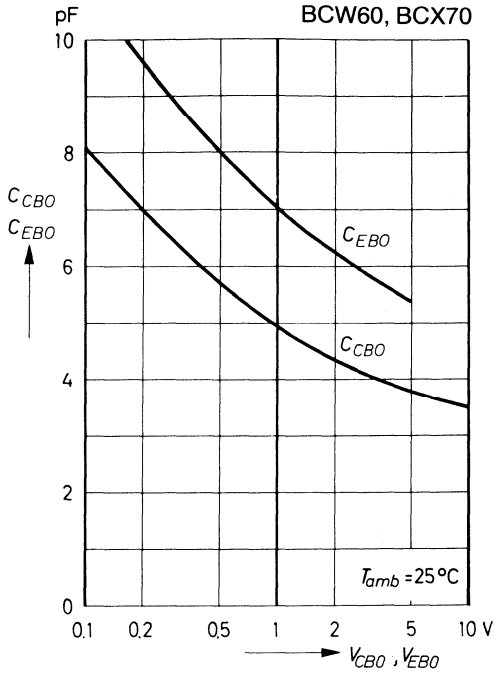
Collector current versus base emitter voltage



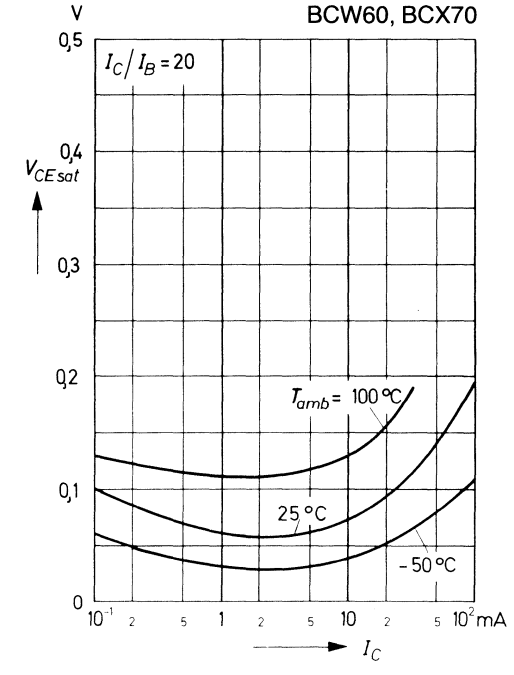
Collector cutoff current versus ambient temperature



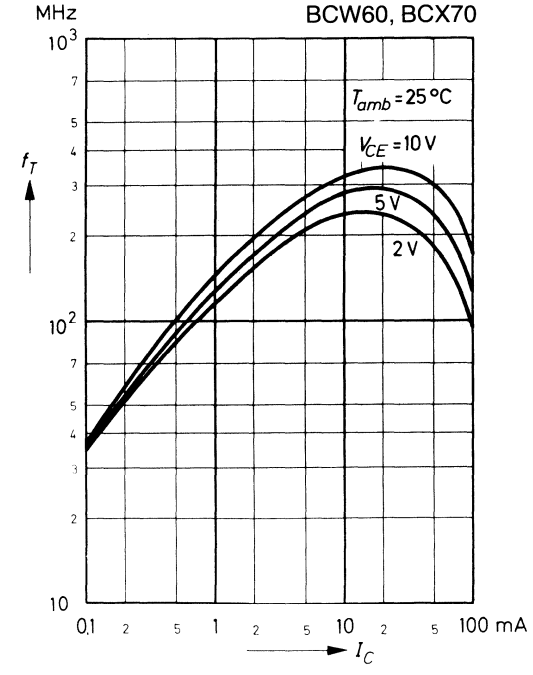
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



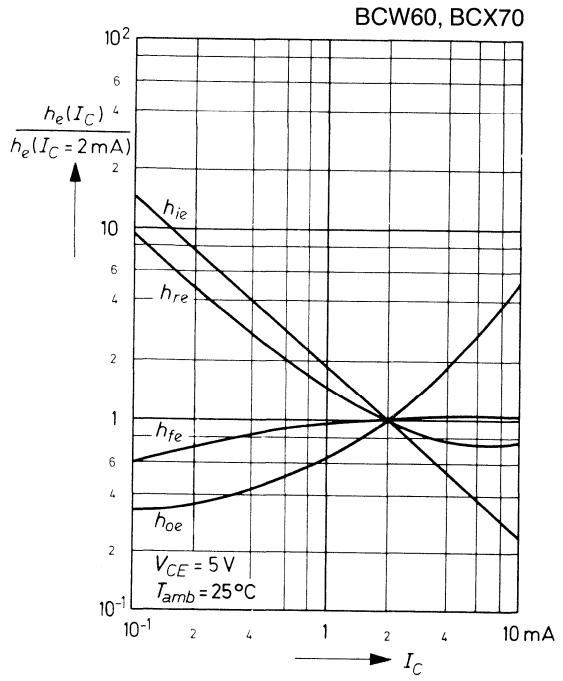
Collector saturation voltage versus collector current



Gain bandwidth product versus collector current



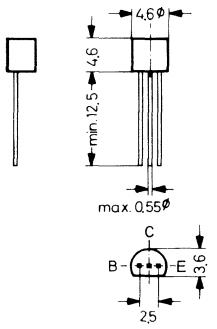
Relative h-parameters versus collector current



JC500, JC501

NPN Silicon Epitaxial Planar Transistors
for switching and amplifier applications

The transistors are subdivided into four groups O, P, Q and R according to their current gain.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**JC501** **JC500**	V_{CES} V_{CES}	50 30	V V
Collector Emitter Voltage	**JC501** **JC500**	V_{CEO} V_{CEO}	45 25	V V
Emitter Base Voltage		V_{EBO}	6	V
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Base Current		I_B	50	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

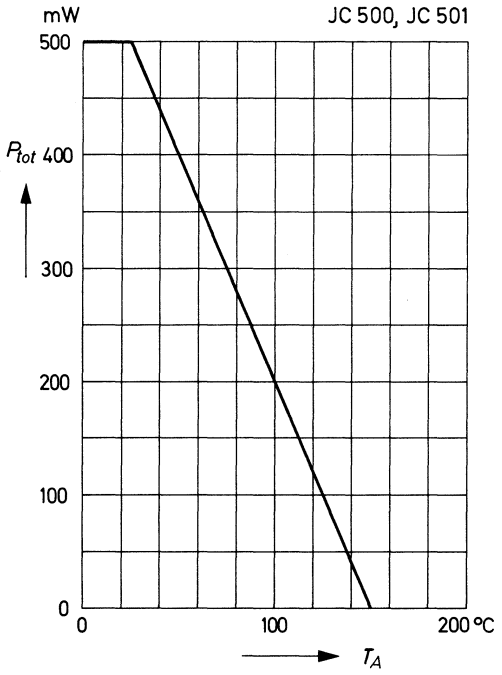
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 5 V, I_C = 1 mA **Current Gain Group O** **P** **Q** **R**	 h_{FE} h_{FE} h_{FE} h_{FE}	 90 135 200 300	 – – – –	 180 270 400 600	 – – – –
Collector Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA at I_C = 100 mA, I_B = 5 mA	 V_{CEsat} V_{CEsat}	 – –	 0.08 0.23	 0.2 0.6	 V V
Base Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA at I_C = 100 mA, I_B = 5 mA	 V_{BEsat} V_{BEsat}	 – –	 0.73 0.87	 1.00 1.05	 V V
Base Emitter Voltage at V_{CE} = 5 V, I_C = 0.1 mA at V_{CE} = 5 V, I_C = 2 mA at V_{CE} = 5 V, I_C = 100 mA	 V_{BE} V_{BE} V_{BE}	 – 0.55 –	 0.55 0.62 0.83	 – 0.7 –	 V V V
Collector Cutoff Current at V_{CE} = 50 V **JC501** at V_{CE} = 30 V **JC500** at V_{CE} = 50 V, T_{amb} = 125 °C **JC501** at V_{CE} = 30 V, T_{amb} = 125 °C **JC500**	 I_{CES} I_{CES} I_{CES} I_{CES}	 – – – –	 0.2 0.2 0.2 0.2	 15 15 4 4	 nA nA µA µA
Collector Emitter Breakdown Voltage at I_C = 2 mA **JC501** **JC500**	 $V_{(BR)CEO}$ $V_{(BR)CEO}$	 45 25	 – –	 – –	 V V
Emitter Base Breakdown Voltage at I_E = 1 µA **JC501** **JC500**	 $V_{(BR)EBO}$ $V_{(BR)EBO}$	 6 5	 – –	 – –	 V V
Gain Bandwidth Product at V_{CE} = 3 V, I_C = 0.5 mA, f = 100 MHz at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz	 f_T f_T	 – 150	 85 250	 – –	 MHz MHz
Collector Base Capacitance at V_{CBO} = 10 V, f = 1 MHz	C_{CBO}	–	3.5	6	pF
Emitter Base Capacitance at V_{EBO} = 0.5 V, f = 1 MHz	C_{EBO}	–	8	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 0.2 mA, R_G = 2 kΩ, f = 1 kHz	F	–	2	10	dB
Thermal Resistance Junction to Ambient	R_{thA}	–	–	250[1)]	K/W

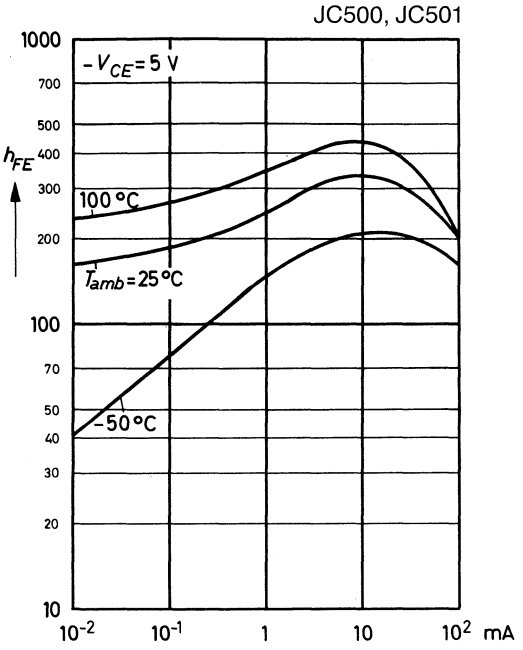
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

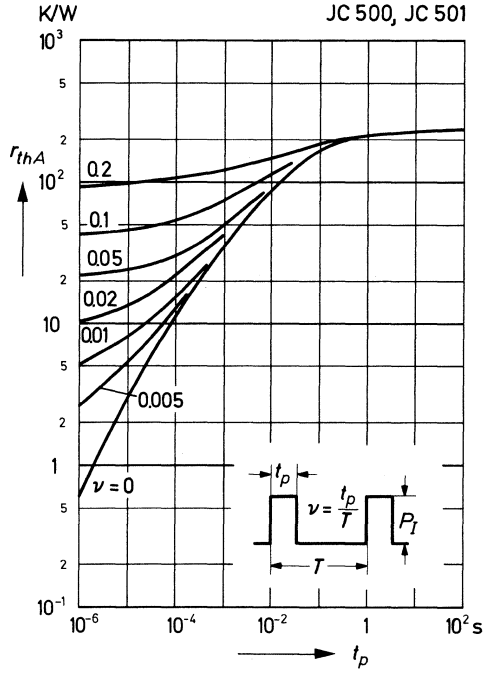


DC current gain versus collector current

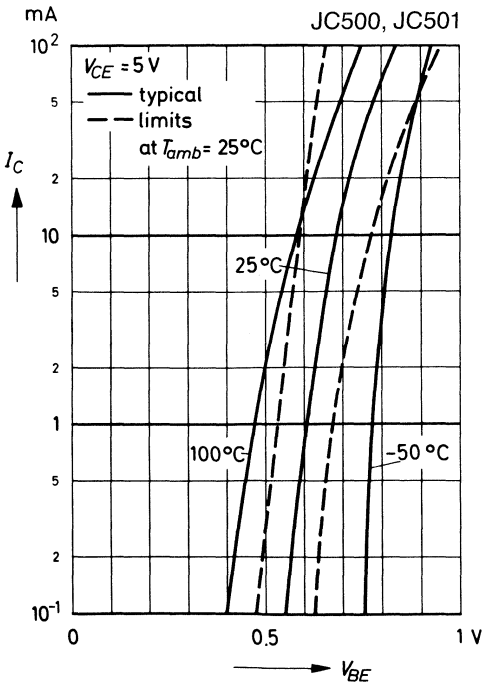


Pulse thermal resistance versus pulse duration

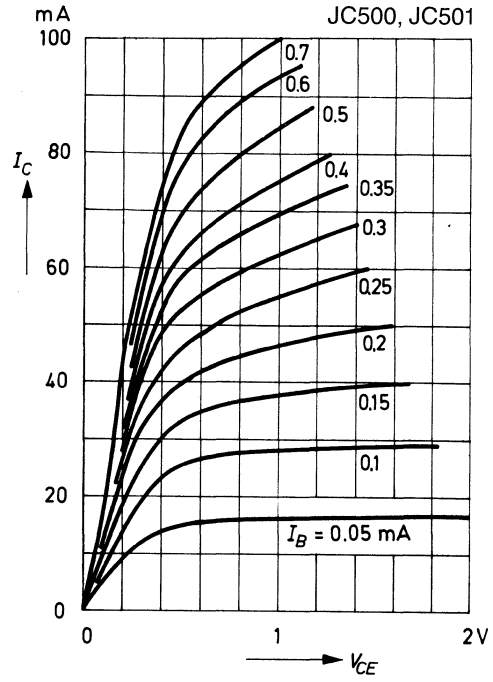
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



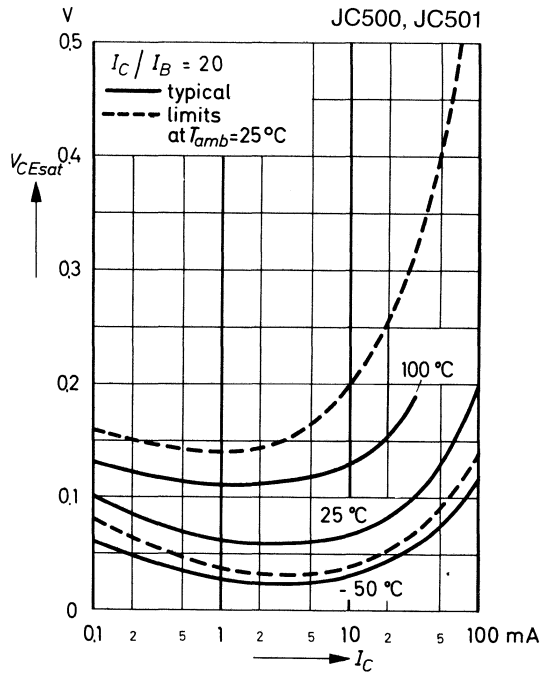
Collector current versus base emitter voltage



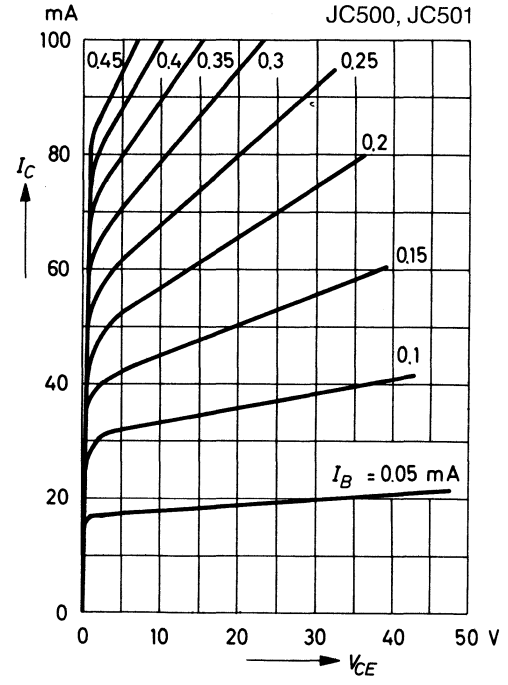
Common emitter collector characteristics



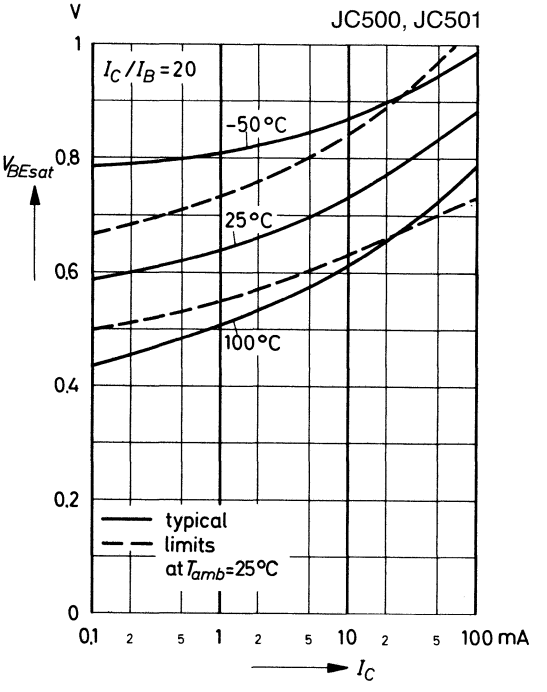
Collector saturation voltage versus collector current



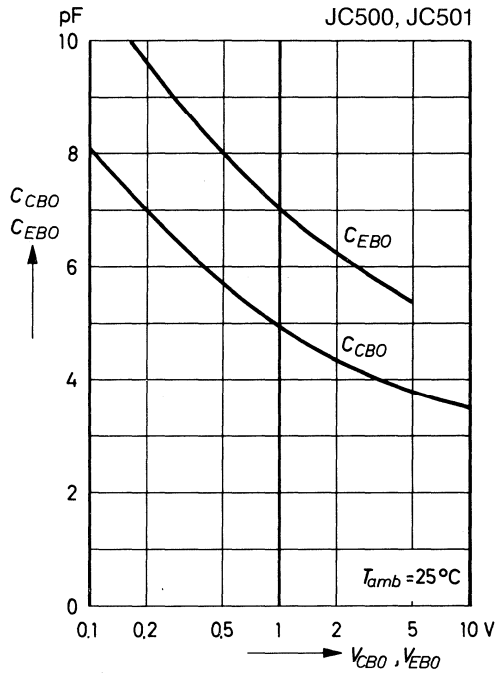
Common emitter collector characteristics



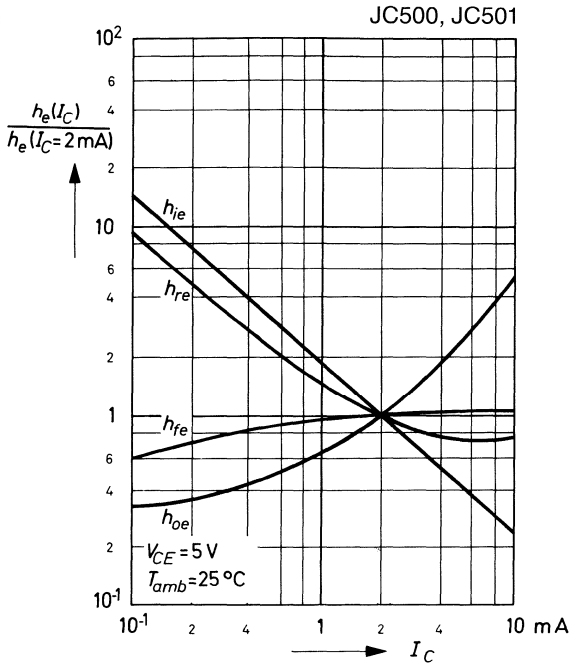
Base saturation voltage versus collector current



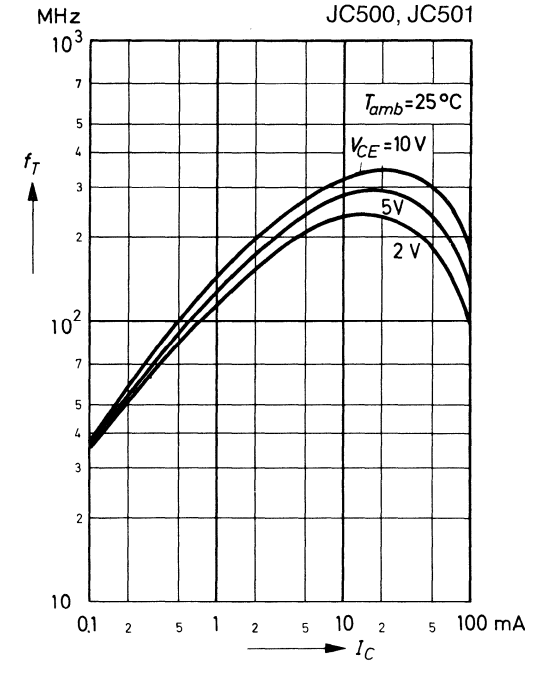
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



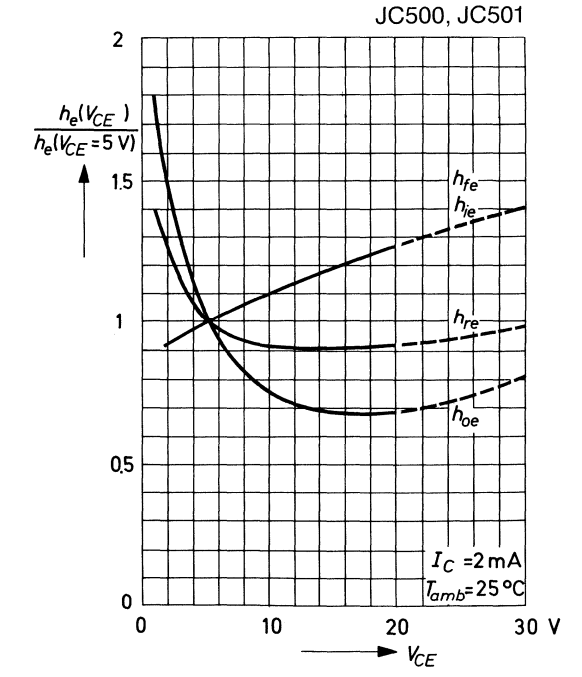
Relative h-parameters versus collector current



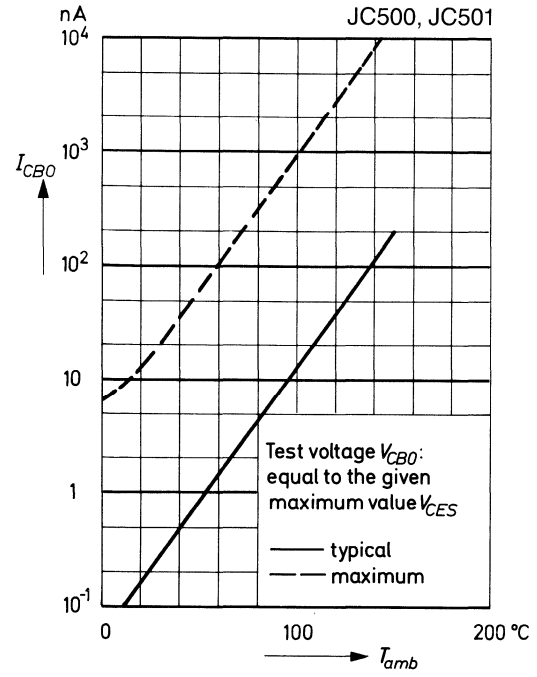
Gain bandwidth product versus collector current



Relative h-parameters versus collector emitter voltage



Collector cutoff current versus ambient temperature



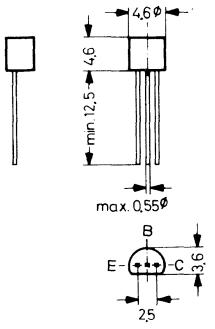
PNP Silicon Transistors

BC250

PNP Silicon Epitaxial Planar Transistor
for switching and amplifier applications

The transistor is subdivided into three groups A, B and C according to its DC current gain.

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector Base Voltage	$-V_{CBO}$	20	V
Collector Emitter Voltage	$-V_{CEO}$	20	V
Emitter Base Voltage	$-V_{EBO}$	5	V
Collector Current	$-I_C$	100	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	300[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

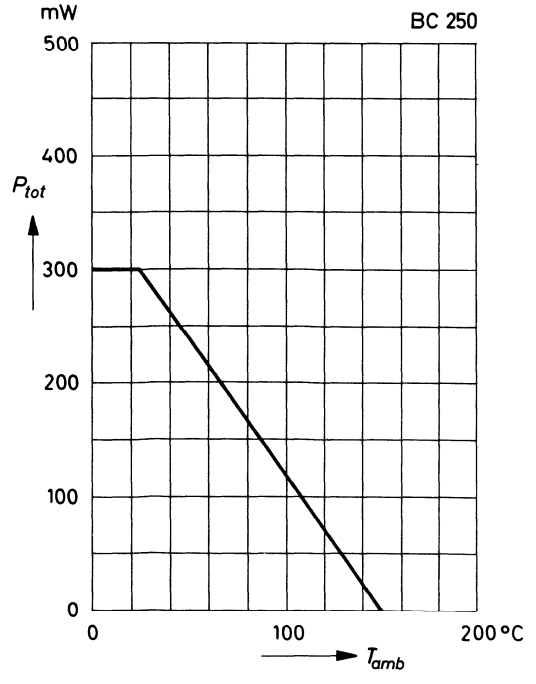
Characteristics at $T_j = 25\ °C$

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE} = 1\ V$, $-I_C = 1\ mA$ **Current Gain Group A** **B** **C**	h_{FE} h_{FE} h_{FE}	35 80 200	– – –	100 250 600	– – –
Collector Saturation Voltage at $-I_C = 30\ mA$, $-I_B = 3\ mA$	$-V_{CEsat}$	–	0.4	–	V
Collector Cutoff Current at $-V_{CB} = 15\ V$	$-I_{CBO}$	–	–	100	nA
Emitter Cutoff Current at $-V_{EB} = 3.8\ V$	$-I_{EBO}$	–	–	100	nA
Gain Bandwidth Product at $-V_{CE} = 5\ V$, $-I_C = 10\ mA$, $f = 100\ MHz$	f_T	–	180	–	MHz
Collector Base Capacitance at $-V_{CBO} = 10\ V$, $f = 1\ MHz$	C_{CBO}	–	3	–	pF
Emitter Base Capacitance at $-V_{EBO} = 0.5\ V$, $f = 1\ MHz$	C_{EBO}	–	12	–	pF
Thermal Resistance Junction to Ambient	R_{thA}	–	–	400[1)]	K/W

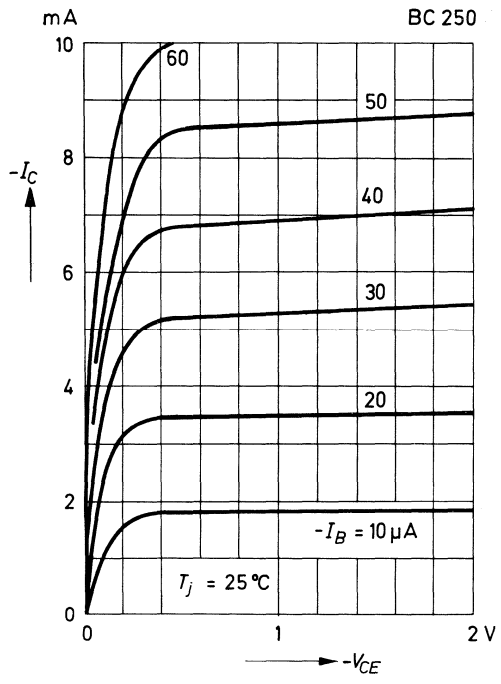
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

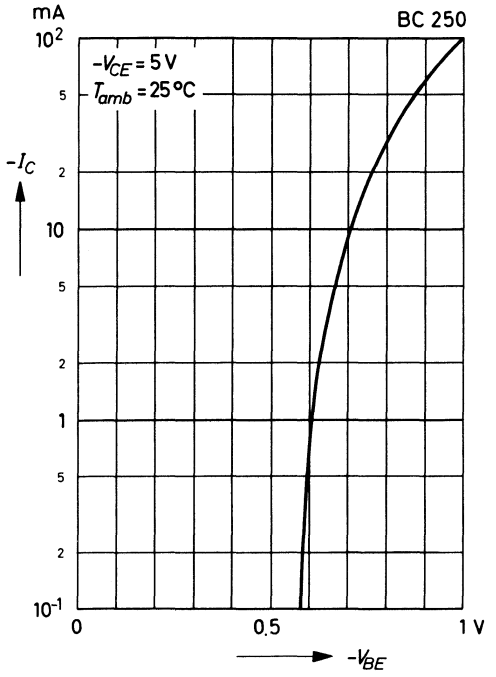
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



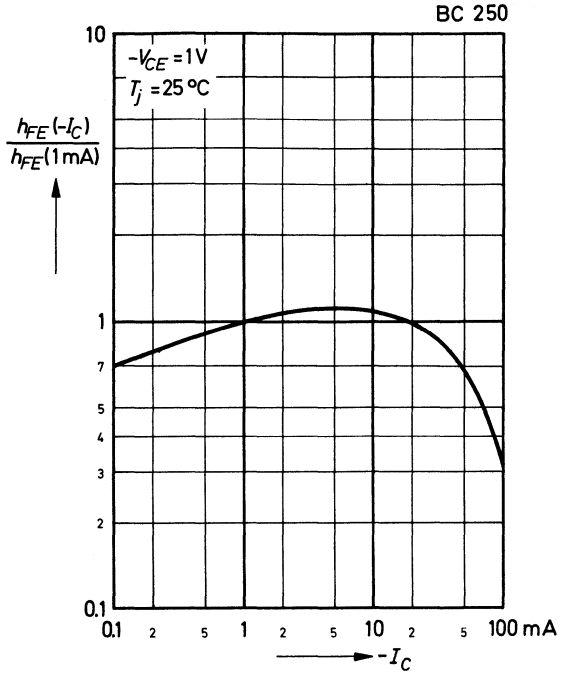
Common emitter collector characteristics



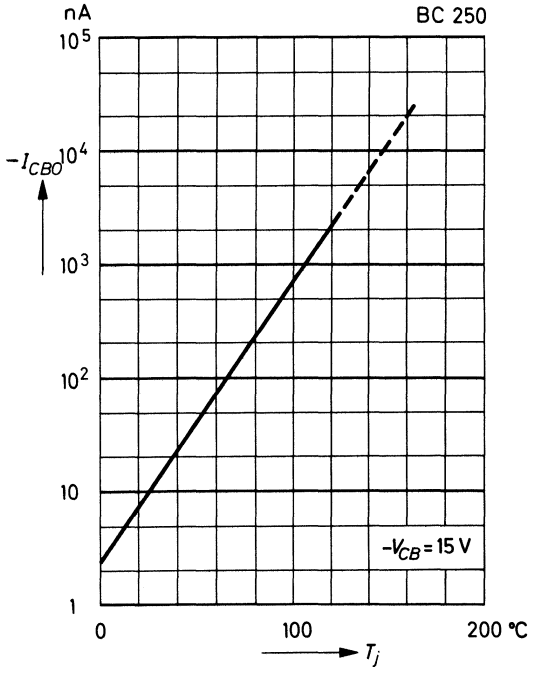
Collector current versus base emitter voltage



Relative DC current gain versus collector current



Collector cutoff current versus junction temperature

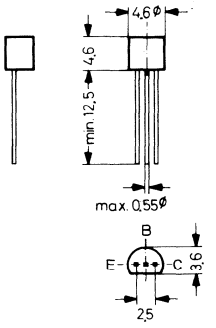


BC327, BC328

PNP Silicon Epitaxial Planar Transistors
for switching and amplifier applications. Especially suitable for AF-driver stages and low power output stages.

These types are also available subdivided into three groups –16, –25 and –40, according to their DC current gain. As complementary types the NPN transistors BC337 and BC338 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC327** **BC328**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector Emitter Voltage	**BC327** **BC328**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	800	mA
Peak Collector Current		$-I_{CM}$	1	A
Base Current		$-I_B$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–55 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

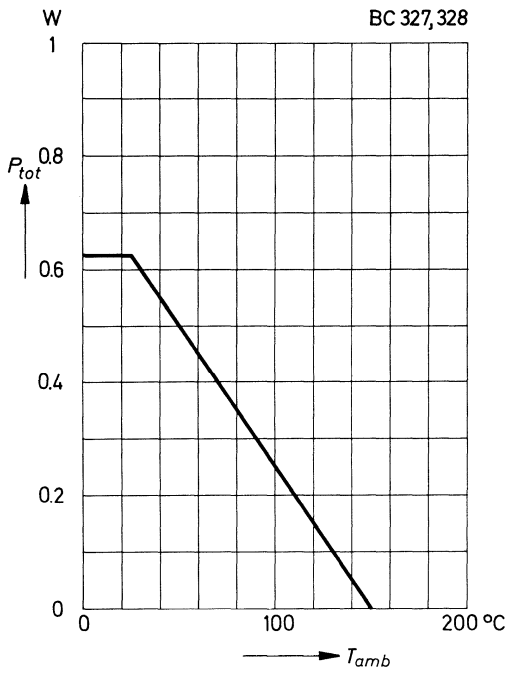
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA **BC327, BC328**	h_{FE}	100	–	630	–
Current Gain Group 16	h_{FE}	100	160	250	–
25	h_{FE}	160	250	400	–
40	h_{FE}	250	400	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA **BC327, BC328**	h_{FE}	60	–	–	–
Current Gain Group 16	h_{FE}	60	130	–	–
25	h_{FE}	100	200	–	–
40	h_{FE}	170	320	–	–
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1)]	K/W
Collector Cutoff Current					
at $-V_{CE}$ = 25 V **BC328**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 45 V **BC327**	$-I_{CES}$	–	2	100	nA
at $-V_{CE}$ = 25 V, T_{amb} =125 °C **BC328**	$-I_{CES}$	–	–	10	μA
at $-V_{CE}$ = 45 V, T_{amb} =125 °C **BC327**	$-I_{CES}$	–	–	10	μA
Collector Emitter Breakdown Voltage					
at $-I_C$ = 10 mA **BC327**	$-V_{(BR)CEO}$	45	–	–	V
BC328	$-V_{(BR)CEO}$	25	–	–	V
Collector Emitter Breakdown Voltage					
at $-I_C$ = 0.1 mA **BC327**	$-V_{(BR)CES}$	50	–	–	V
BC328	$-V_{(BR)CES}$	30	–	–	V
Emitter Base Breakdown Voltage at $-I_E$ = 0.1 mA	$-V_{(BR)EBO}$	5	–	–	V
Collector Saturation Voltage at $-I_C$ = 500mA, $-I_B$ = 50 mA	$-V_{CEsat}$	–	–	0.7	V
Base Emitter Voltage at $-V_{CE}$ = 1V, $-I_C$ = 300 mA	$-V_{BE}$	–	–	1.2	V
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	100	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz	C_{CBO}	–	12	–	pF

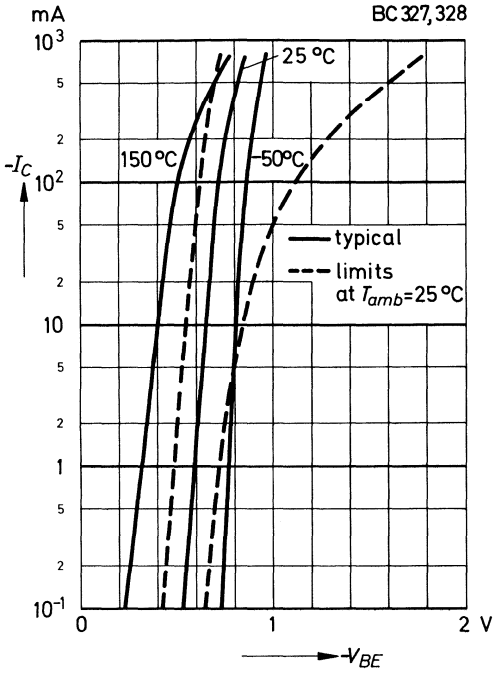
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

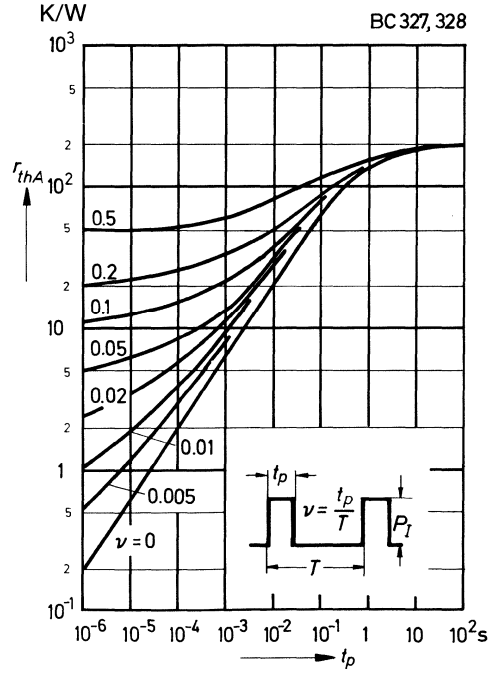


Collector current versus base emitter voltage

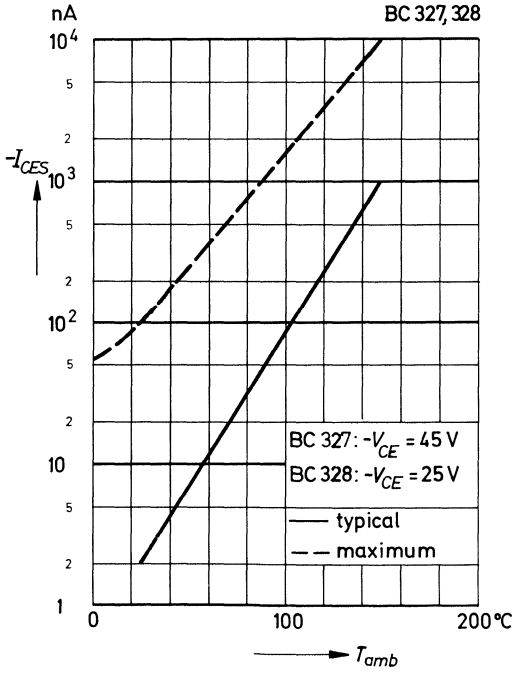


Pulse thermal resistance versus pulse duration

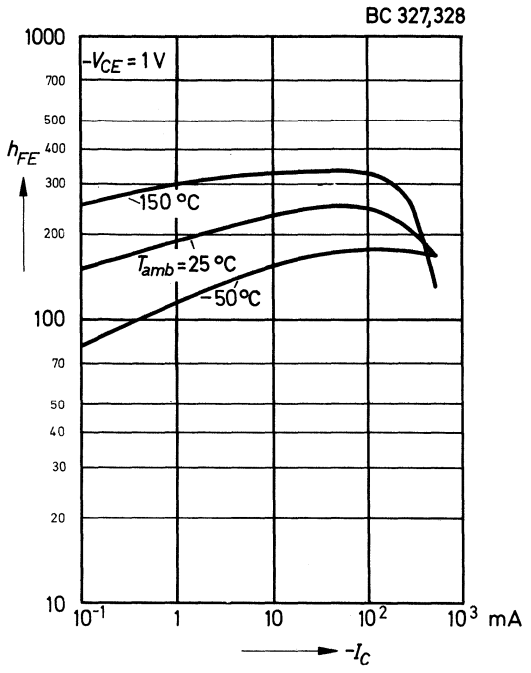
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



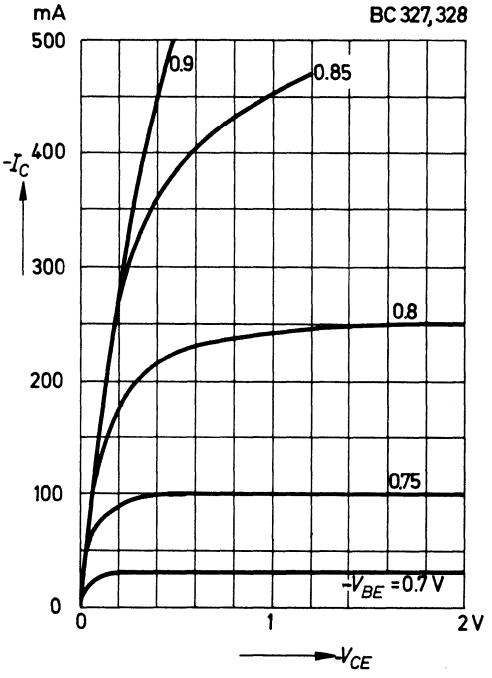
Collector cutoff current versus ambient temperature



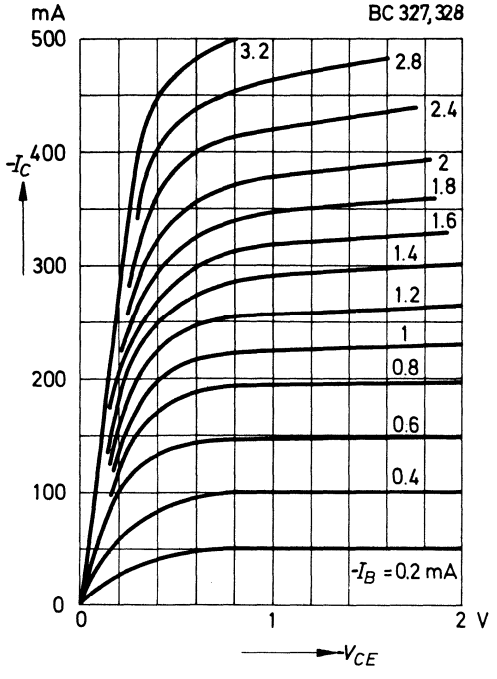
DC current gain versus collector current



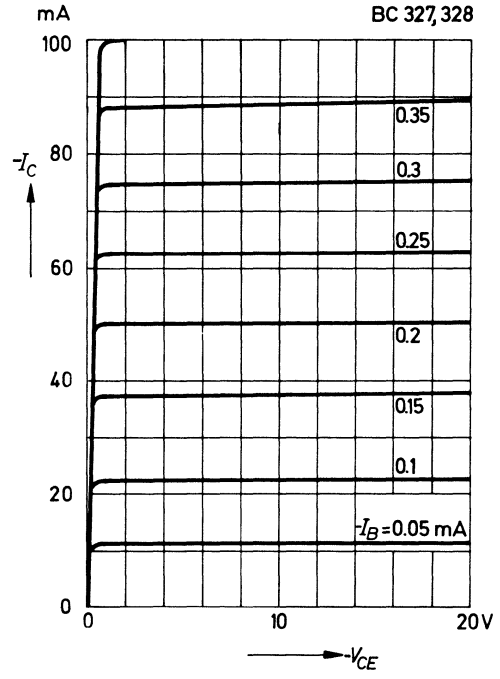
Common emitter collector characteristics



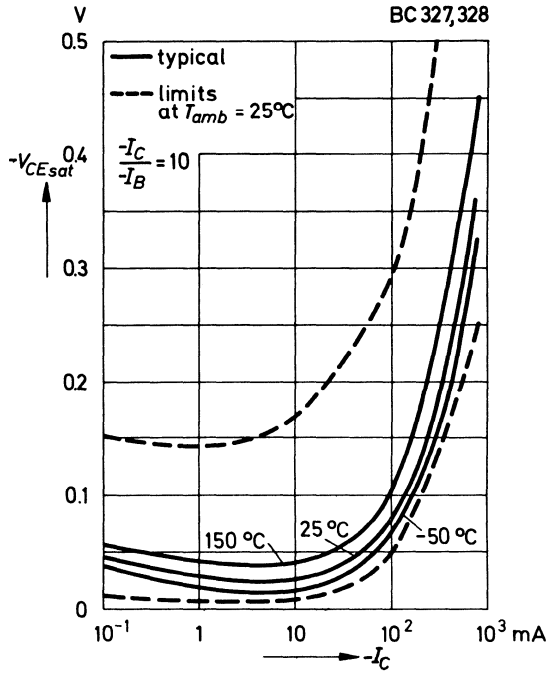
Common emitter collector characteristics



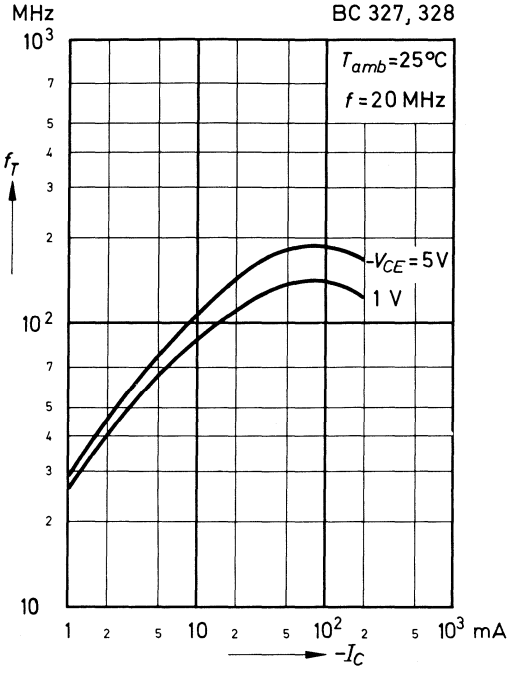
Common emitter collector characteristics



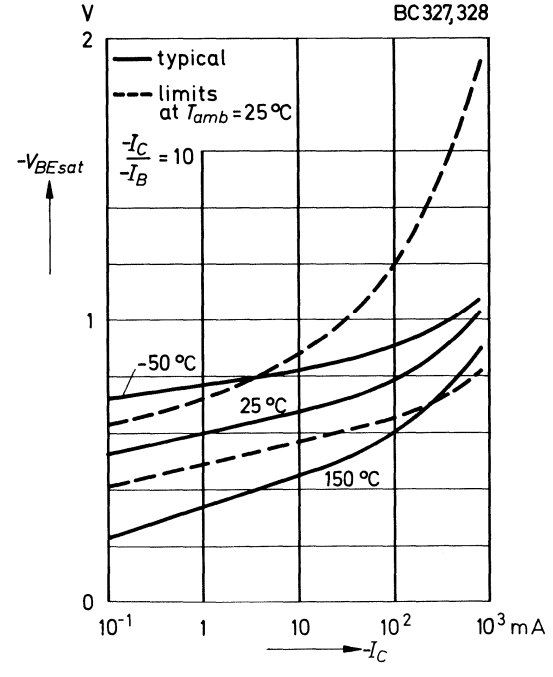
Collector saturation voltage versus collector current



Gain bandwith product versus collector current



Base saturation voltage versus collector current

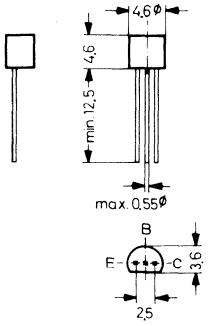


BC415, BC416

PNP Silicon Epitaxial Planar Transistors
for use in high-quality, low noise AF and DC amplifiers.

These types are subdivided into three groups A, B and C, according to their DC current gain. As complementary types the NPN transistors BC413 and BC414 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC415**	$-V_{CBO}$	45	V
	BC416	$-V_{CBO}$	50	V
Collector Emitter Voltage	**BC415**	$-V_{CEO}$	30	V
	BC416	$-V_{CEO}$	45	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Base Current		$-I_B$	20	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

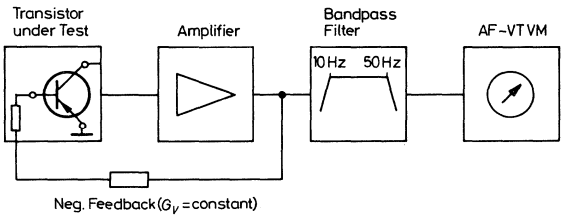
Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz						
Small Signal Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio	**Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at $-V_{CE}$ = 5 V, $-I_C$ = 0.01 mA	**Current Gain Group A**	h_{FE}	40	90	–	–
	B	h_{FE}	100	150	–	–
	C	h_{FE}	100	270	–	–
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA	**Current Gain Group A**	h_{FE}	120	170	220	–
	B	h_{FE}	180	290	460	–
	C	h_{FE}	380	500	800	–
Thermal Resistance Junction to Ambient		R_{thA}	–	–	250[1]	K/W
Collector Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA		$-V_{CEsat}$	–	0.075	0.25	V
at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{CEsat}$	–	0.25	0.6	V
Base Saturation Voltage at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{BEsat}$	–	0.9	–	V
Base Emitter Voltage						
at $-V_{CE}$ = 5 V, $-I_C$ = 0.01 mA		$-V_{BE}$	–	0.52	–	V
at $-V_{CE}$ = 5 V, $-I_C$ = 0.1 mA		$-V_{BE}$	–	0.55	–	V
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA		$-V_{BE}$	0.55	0.65	0.75	V
Collector Cutoff Current						
at $-V_{CB}$ = 30 V		$-I_{CBO}$	–	–	15	nA
at $-V_{CB}$ = 30 V, T_A = 150 °C		$-I_{CBO}$	–	–	5	μA
Emitter Cutoff Current at $-V_{EB}$ = 4 V		$-I_{EBO}$	–	–	15	nA
Collector Emitter Breakdown Voltage						
at $-I_C$ = 10 mA	**BC415**	$-V_{(BR)CEO}$	30	–	–	V
	BC416	$-V_{(BR)CEO}$	45	–	–	V
Collector Base Breakdown Voltage						
at $-I_C$ = 10 μA	**BC415**	$-V_{(BR)CBO}$	45	–	–	V
	BC416	$-V_{(BR)CBO}$	50	–	–	V
Emitter Base Breakdown Voltage at $-I_{EB}$ = 10 μA		$-V_{(BR)EBO}$	5	–	–	V
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 100 MHz		f_T	–	200	–	MHz
Collector Base Capacitance at $-V_{CBO}$ = 10 V, f = 1 MHz		C_{CBO}	–	4.5	–	pF

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics, continuation

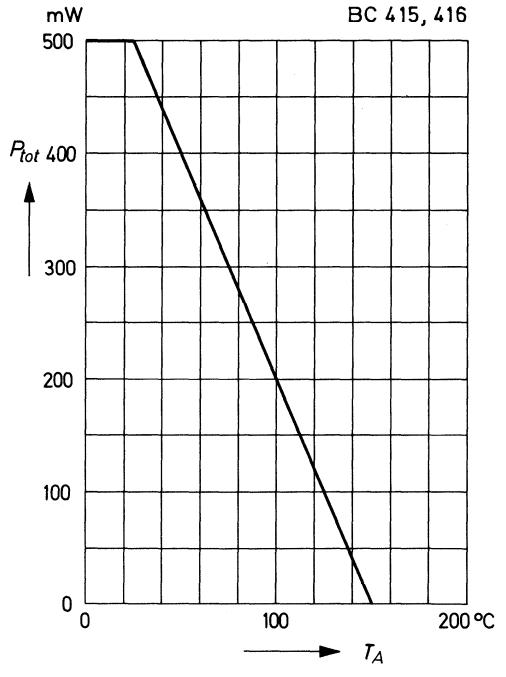
	Symbol	Min.	Typ.	Max.	Unit
Noise Figure at $-V_{CE} = 5$ V, $-I_C = 0.2$ mA, $R_G = 2$ kΩ, f = 30 Hz . . . 15 kHz	F	–	–	2	dB
Equivalent Noise EMF referred to base at $-V_{CE} = 5$ V, $-I_C = 0.2$ mA, $R_G = 2$ kΩ, f = 10 . . . 50 Hz	v_r	–	–	0.11	μV



Test circuit for equivalent noise EMF

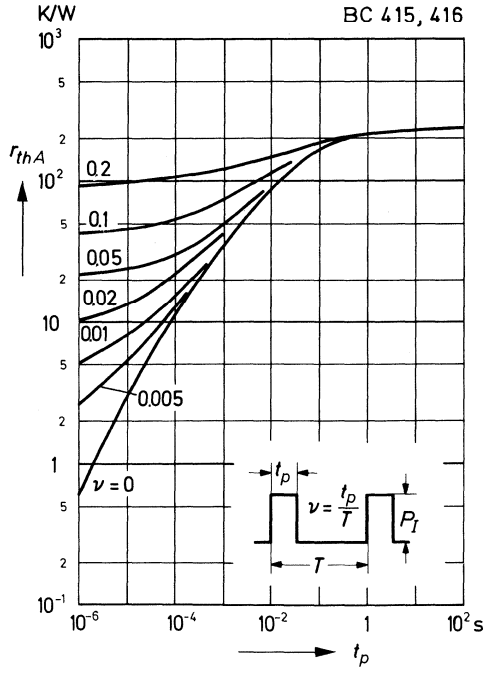
Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

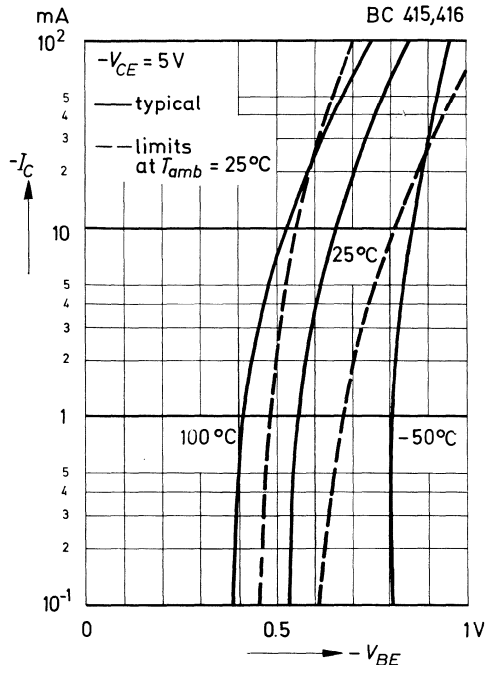


Pulse thermal resistance versus pulse duration

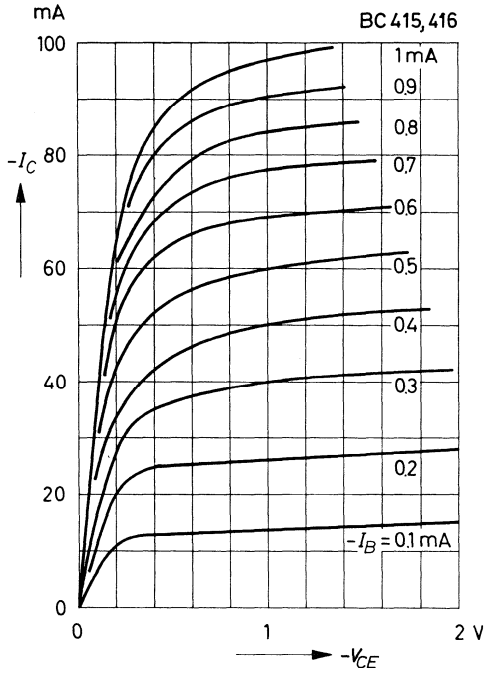
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



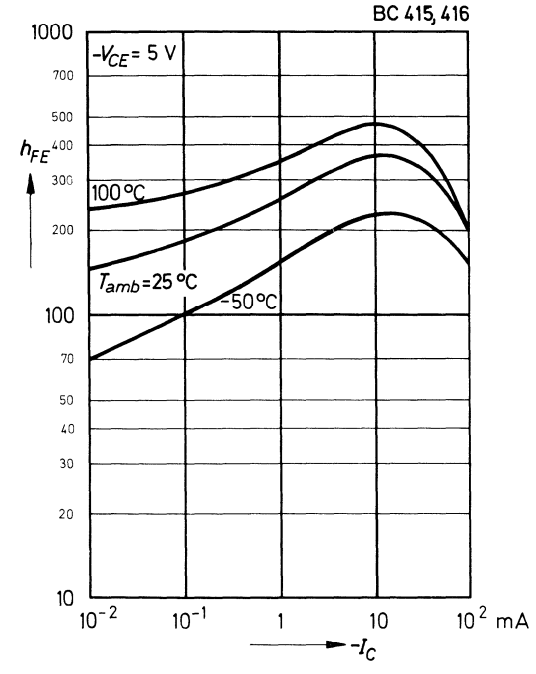
Collector current versus base emitter voltage



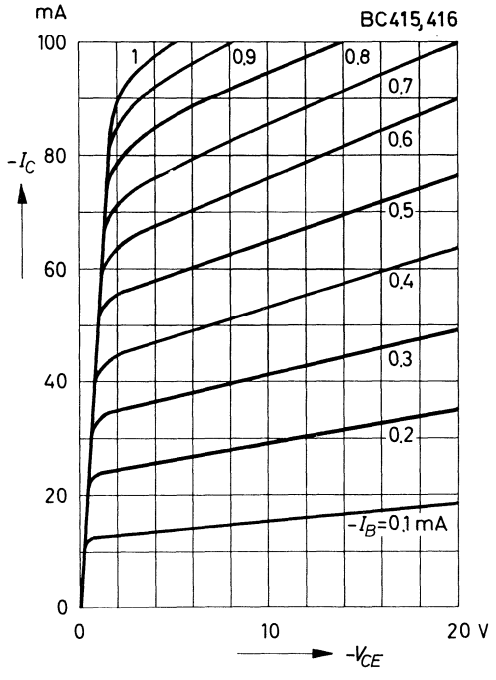
Common emitter collector characteristics



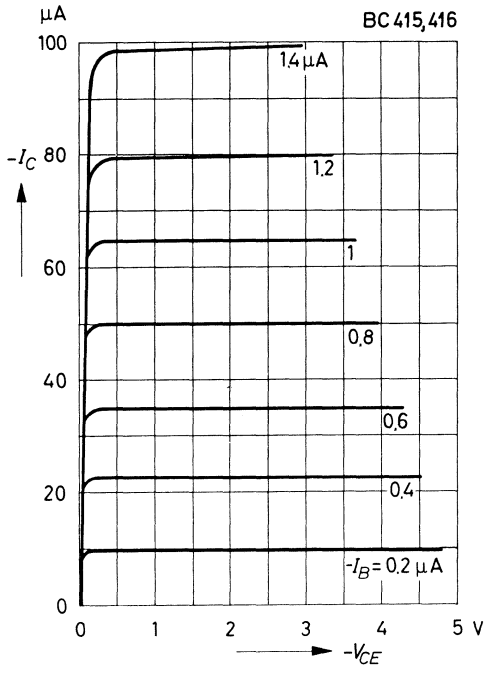
DC current gain versus collector current



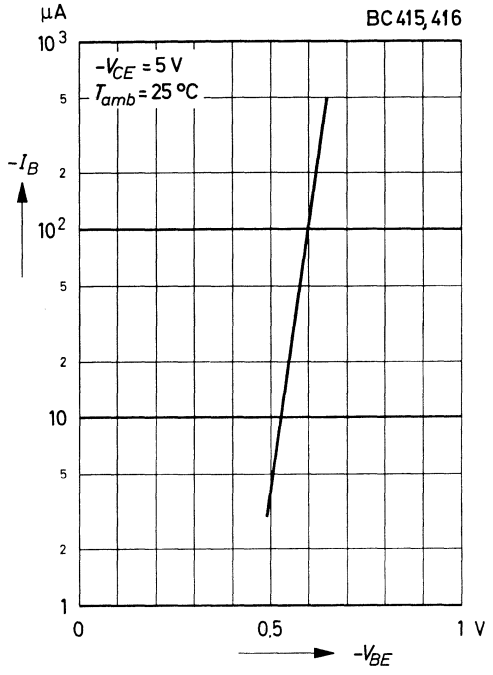
Common emitter collector characteristics



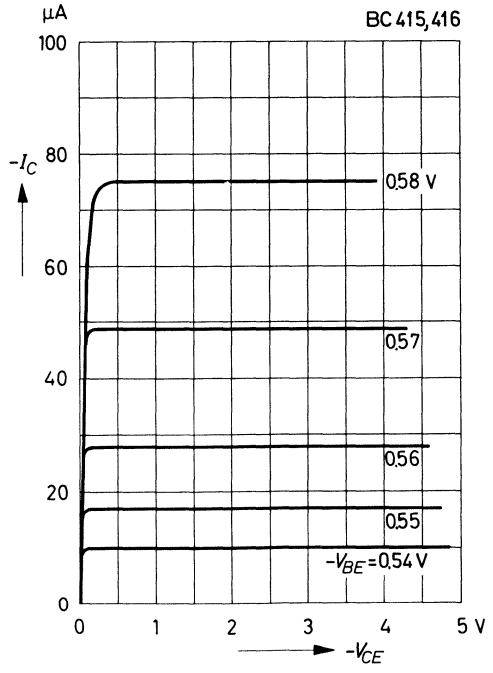
Common emitter collector characteristics



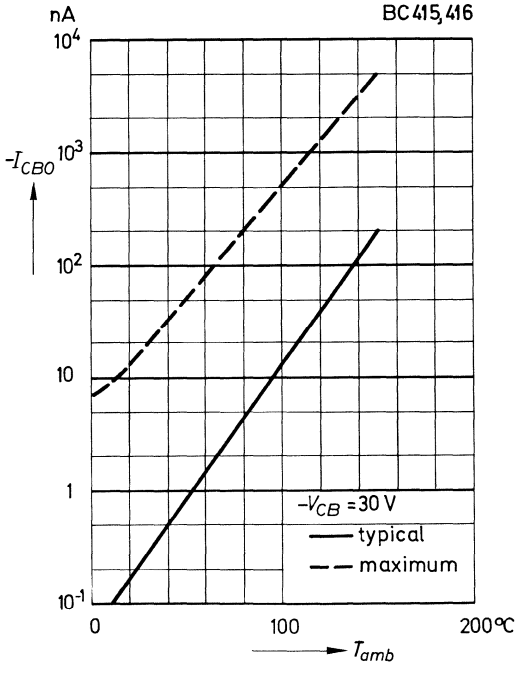
Common emitter input characteristic



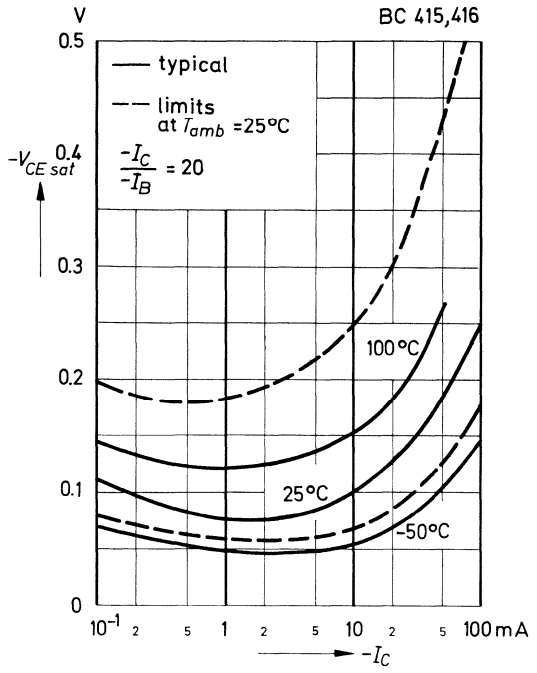
Common emitter collector characteristics



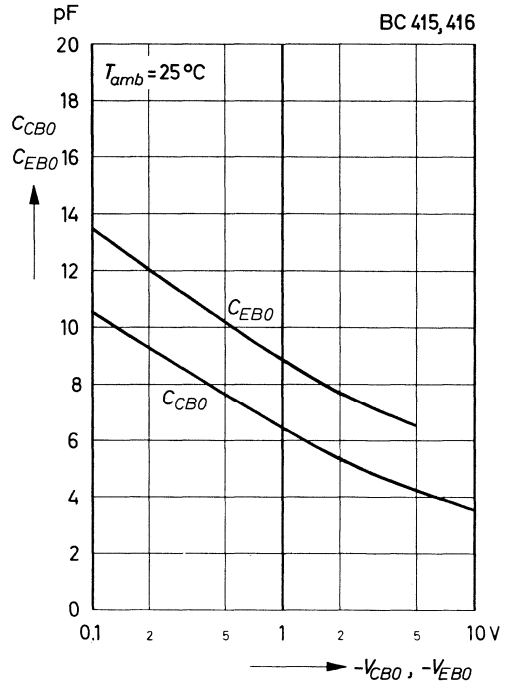
Collector cutoff current versus ambient temperature



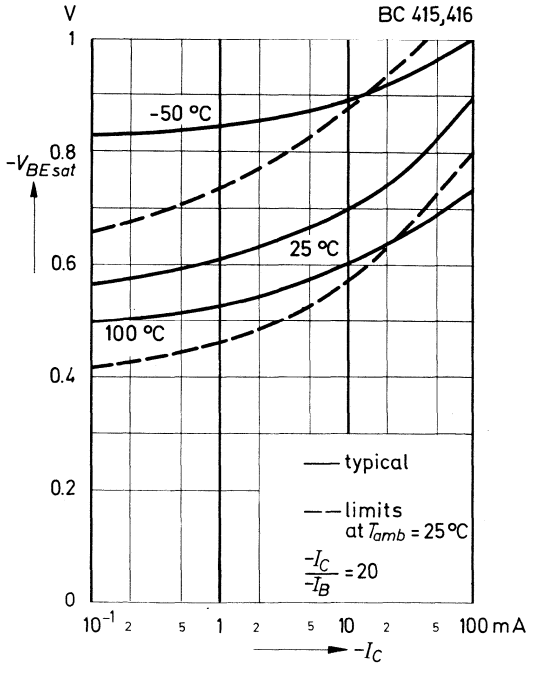
Collector saturation voltage versus collector current



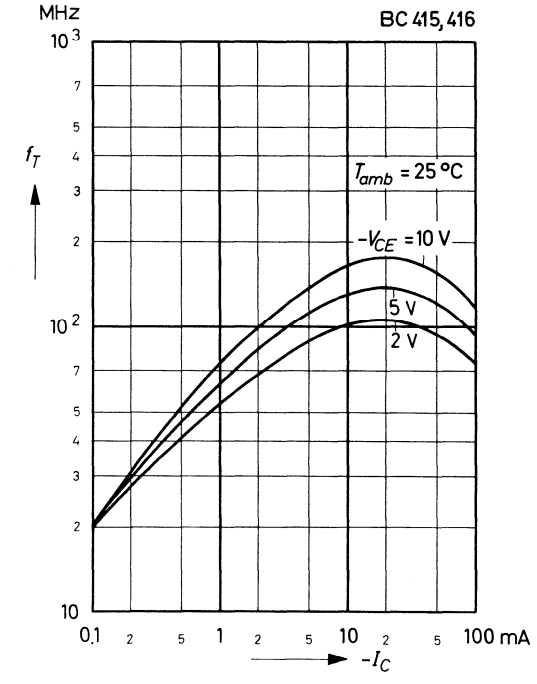
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



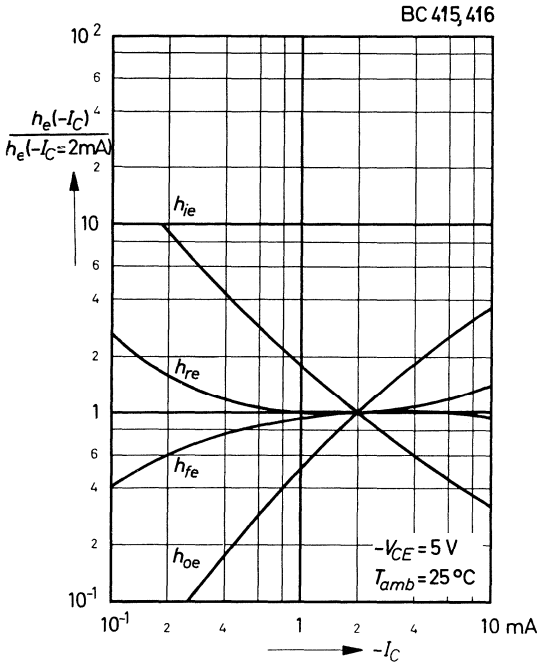
Base saturation voltage versus collector current



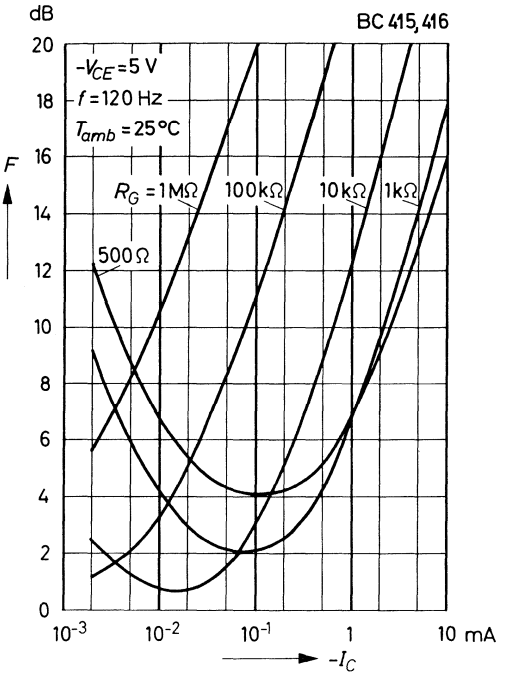
Gain bandwidth product versus collector current



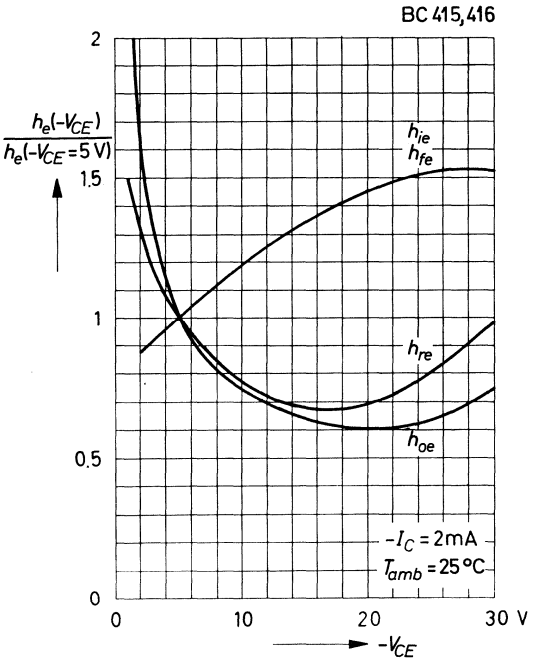
Relative h-parameters versus collector current



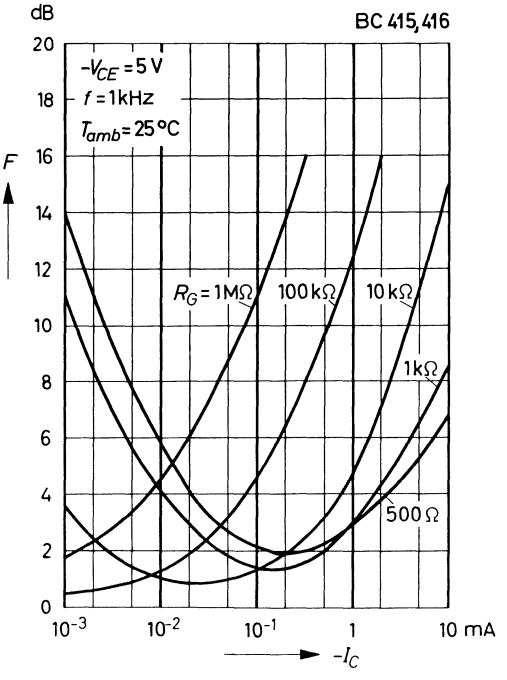
Noise figure versus collector current



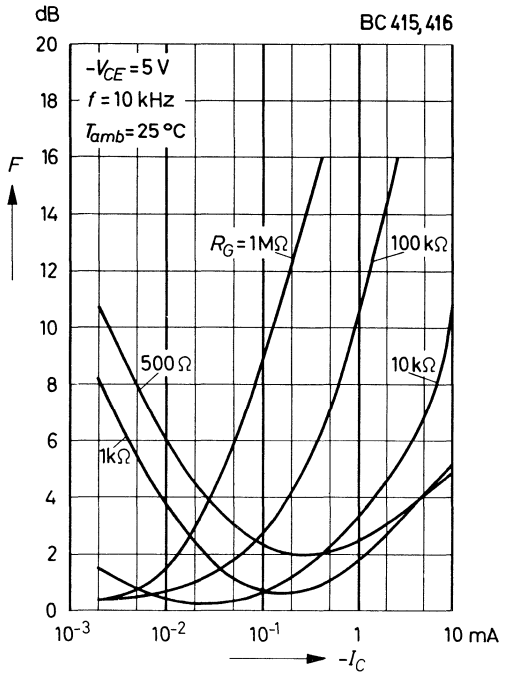
Relative h-parameters versus collector emitter voltage



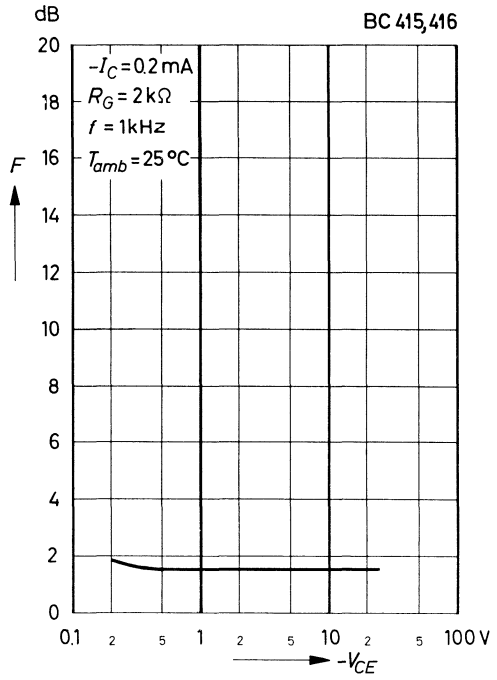
Noise figure versus collector current



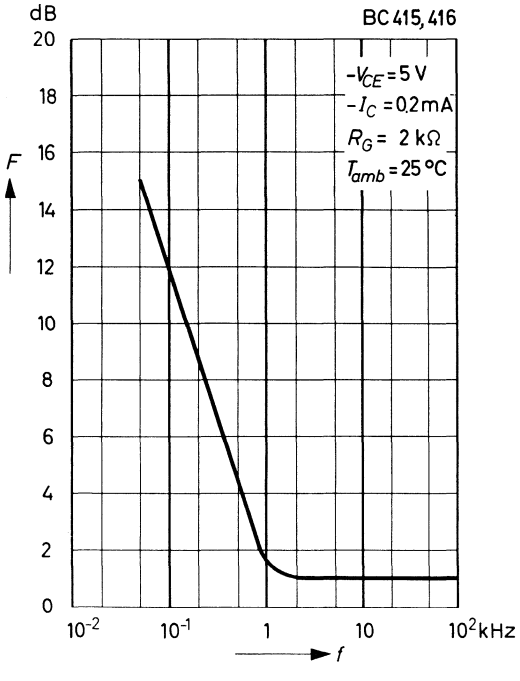
Noise figure versus collector current



Noise figure versus collector emitter voltage



Noise figure versus frequency

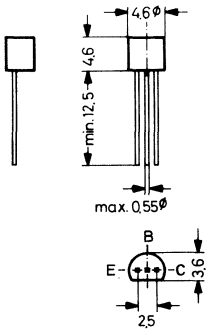


BC446, BC448, BC450

PNP Silicon Epitaxial Planar Transistors
for high voltage drivers and output stages.

As complementary types the NPN transistors BC445, BC447 and BC449 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC446**	$-V_{CBO}$	60	V
	BC448	$-V_{CBO}$	80	V
	BC450	$-V_{CBO}$	100	V
Collector Emitter Voltage	**BC446**	$-V_{CEO}$	60	V
	BC448	$-V_{CEO}$	80	V
	BC450	$-V_{CEO}$	100	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	300	mA
Power Dissipation at $T_{amb} = 25$ °C		P_{tot}	625[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 ... +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at $T_{amb} = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain					
at $-V_{CE} = 5$ V, $-I_C = 2$ mA	h_{FE}	50	–	460	–
Current Gain Group A	h_{FE}	120	–	220	–
Current Gain Group B (only BC446, BC448)	h_{FE}	180	–	460	–
at $-V_{CE} = 5$ V, $-I_C = 10$ mA	h_{FE}	50	–	–	–
Current Gain Group A	h_{FE}	100	–	–	–
Current Gain Group B (only BC446, BC448)	h_{FE}	160	–	–	–
at $-V_{CE} = 5$ V, $-I_C = 100$ mA	h_{FE}	50	–	–	–
Current Gain Group A	h_{FE}	60	–	–	–
Current Gain Group B (only BC446, BC448)	h_{FE}	90	–	–	–
Thermal Resistance Junction to Ambient	R_{thA}	–	–	200[1]	K/W
Collector Saturation Voltage at $-I_C = 100$ mA, $-I_B = 10$ mA	$-V_{CEsat}$	–	0.125	0.25	V
Base Saturation Voltage at $-I_C = 100$ mA, $-I_B = 10$ mA	$-V_{BEsat}$	–	0.85	–	V
Base Emitter Voltage at $-V_{CE} = 5$ V, $-I_C = 100$ mA	$-V_{BE}$	–	0.76	1.2	V
Collector Emitter Breakdown Voltage					
at $-I_C = 1$ mA **BC446**	$-V_{(BR)CEO}$	60	–	–	V
BC448	$-V_{(BR)CEO}$	80	–	–	V
BC450	$-V_{(BR)CEO}$	100	–	–	V
Collector Base Breakdown Voltage					
at $-I_C = 100$ µA **BC446**	$-V_{(BR)CBO}$	60	–	–	V
BC448	$-V_{(BR)CBO}$	80	–	–	V
BC450	$-V_{(BR)CBO}$	100	–	–	V
Emitter Base Breakdown Voltage at $-I_E = 10$ µA	$-V_{(BR)EBO}$	4	–	–	V
Collector Cutoff Current					
at $-V_{CB} = 30$ V **BC446**	$-I_{CBO}$	–	–	100	nA
at $-V_{CB} = 40$ V **BC448**	$-I_{CBO}$	–	–	100	nA
at $-V_{CB} = 60$ V **BC450**	$-I_{CBO}$	–	–	100	nA
Gain Bandwidth Product at $-V_{CE} = 5$ V, $-I_C = 50$ mA, $f = 100$ MHz	f_T	100	200	–	MHz
Collector Base Capacitance at $-V_{CB} = 10$ V, $f = 1$ MHz	C_{CBO}	–	3	–	pF
Emitter Base Capacitance at $-V_{EB} = 0.5$ V, $f = 1$ MHz	C_{EBO}	–	20	–	pF

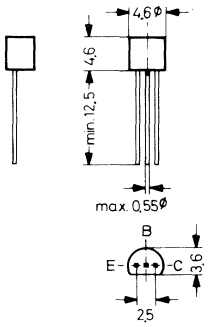
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

BC556 ... BC560

PNP Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC556 is available in groups A and B, however, the types BC557, BC558, BC559 and BC560 can be supplied in all three groups. The BC559 and BC560 are low noise types. As complementary types the NPN transistors BC546 . . . BC550 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC556**	$-V_{CBO}$	80	V
	BC557, BC560	$-V_{CBO}$	50	V
	BC558, BC559	$-V_{CBO}$	30	V
Collector Emitter Voltage	**BC556**	$-V_{CES}$	80	V
	BC557, BC560	$-V_{CES}$	50	V
	BC558, BC559	$-V_{CES}$	30	V
Collector Emitter Voltage	**BC556**	$-V_{CEO}$	65	V
	BC557, BC560	$-V_{CEO}$	45	V
	BC558, BC559	$-V_{CEO}$	30	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Peak Collector Current		$-I_{CM}$	200	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	200	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	–65 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz						
Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio	**Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at $-V_{CE}$ = 5 V, $-I_C$ = 10 μA	**Current Gain Group A**	h_{FE}	–	90	–	–
	B	h_{FE}	–	150	–	–
	C	h_{FE}	–	270	–	–
at $-V_{CE}$ =5 V, $-I_C$ = 2 mA	**Current Gain Group A**	h_{FE}	110	180	220	–
	B	h_{FE}	200	290	450	–
	C	h_{FE}	420	500	800	–
at $-V_{CE}$ = 5 V, $-I_C$ = 100 mA	**Current Gain Group A**	h_{FE}	–	120	–	–
	B	h_{FE}	–	200	–	–
	C	h_{FE}	–	400	–	–
Thermal Resistance Junction to Ambient		R_{thA}	–	–	250[1]	K/W
Collector Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA		$-V_{CEsat}$	–	80	300	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{CEsat}$	–	250	650	mV
Base Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA		$-V_{BEsat}$	–	700	–	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{BEsat}$	–	900	–	mV
Base Emitter Voltage						
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA		$-V_{BE}$	600	660	750	mV
at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA		$-V_{BE}$	–	–	800	mV
Collector Cutoff Current						
at $-V_{CE}$ = 80 V	**BC556**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 50 V	**BC557, BC560**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 30 V	**BC558, BC559**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 80 V, T_j = 125 °C	**BC556**	$-I_{CES}$	–	–	4	μA
at $-V_{CE}$ = 50 V, T_j = 125 °C	**BC557, BC560**	$-I_{CES}$	–	–	4	μA
at $-V_{CE}$ = 30 V, T_j = 125 °C	**BC558, BC559**	$-I_{CES}$	–	–	4	μA
at $-V_{CB}$ = 30 V		$-I_{CBO}$	–	–	15	nA
at $-V_{CB}$ = 30 V, T_j = 150 °C		$-I_{CBO}$	–	–	5	μA
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 100 MHz		f_T	–	150	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz		C_{CBO}	–	–	6	pF

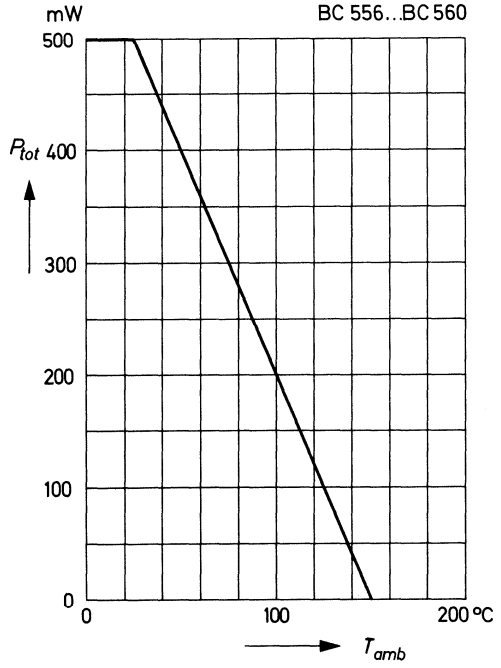
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics, continuation

		Symbol	Min.	Typ.	Max.	Unit
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f= 1 kHz, △f = 200 Hz	**BC556, BC557, BC558**	F	–	2	10	dB
	BC559, BC560	F	–	1	4	dB
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f = 30 . . . 15000 Hz	**BC559**	F	–	1.2	4	dB
	BC560	F	–	1.2	2	dB
Equivalent Noise EMF at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f = 10 . . . 50 Hz	**BC560**	v_r	–	–	0.11	μV

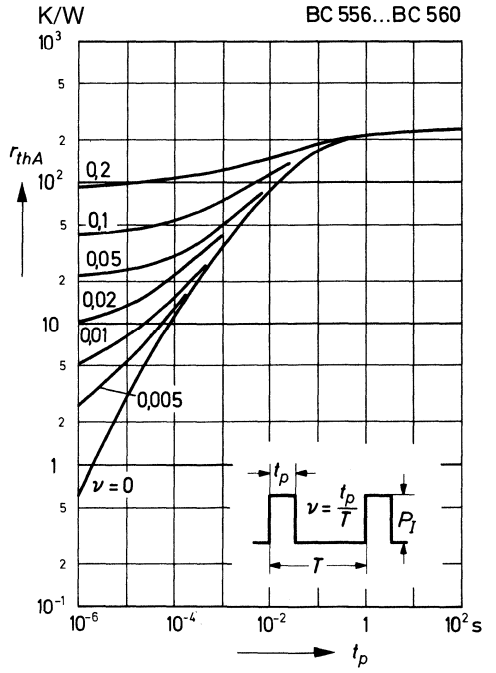
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

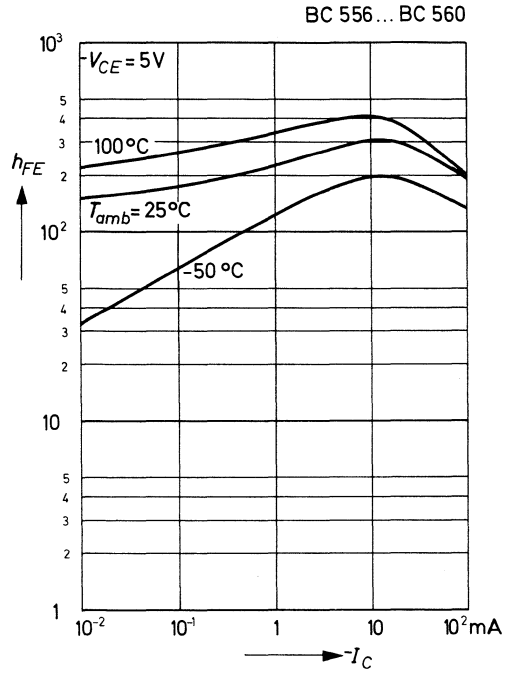


Pulse thermal resistance versus pulse duration

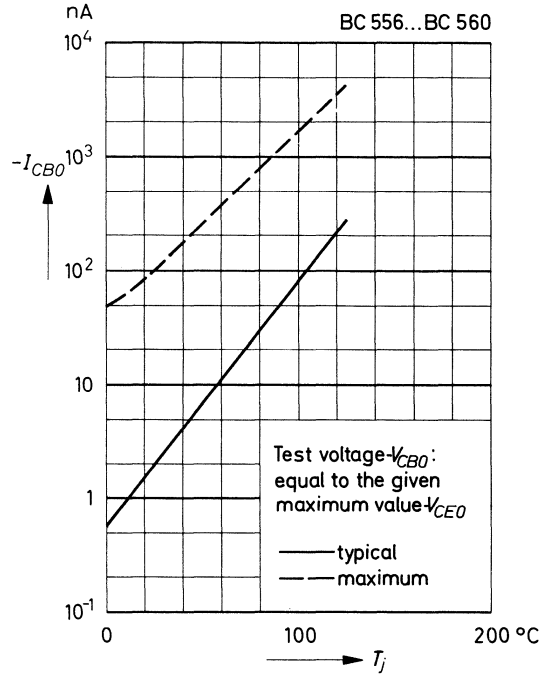
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



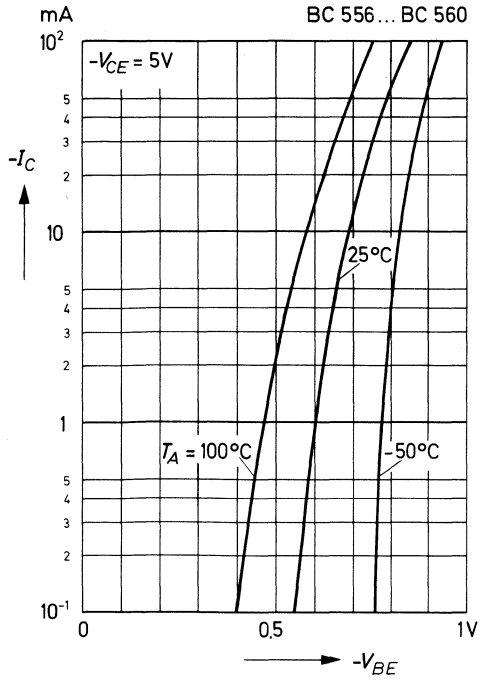
DC current gain versus collector current



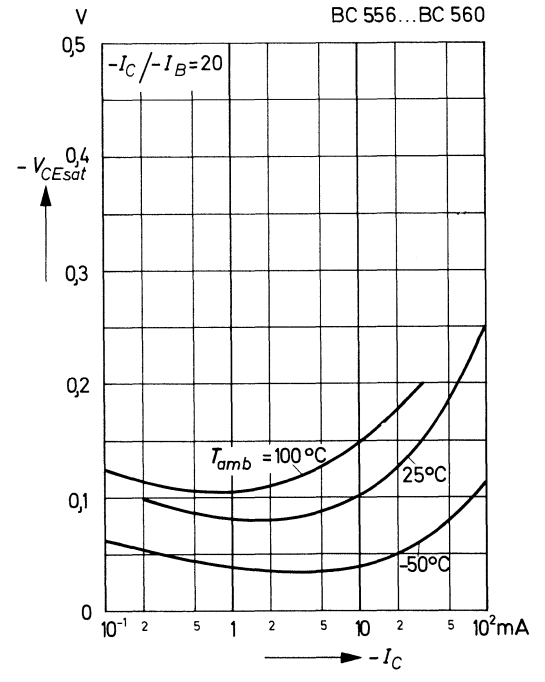
Collector cutoff current versus junction temperature



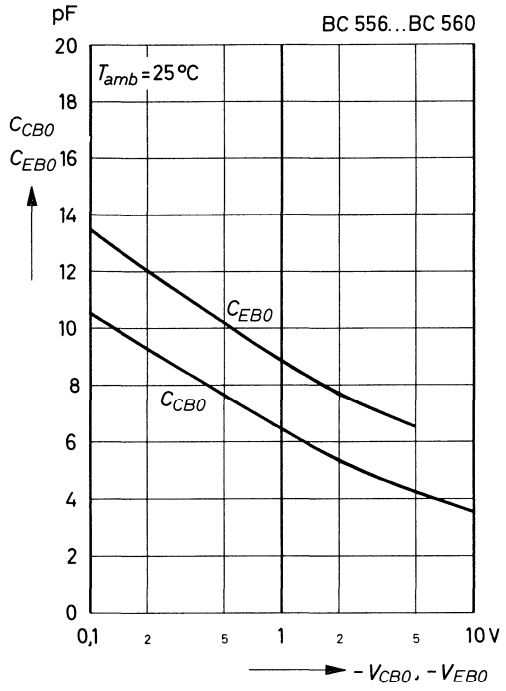
Collector current versus base emitter voltage



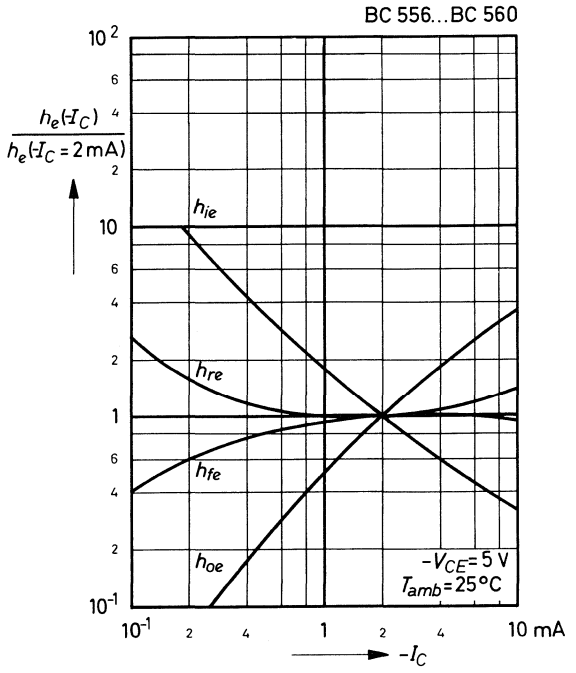
Collector saturation voltage versus collector current



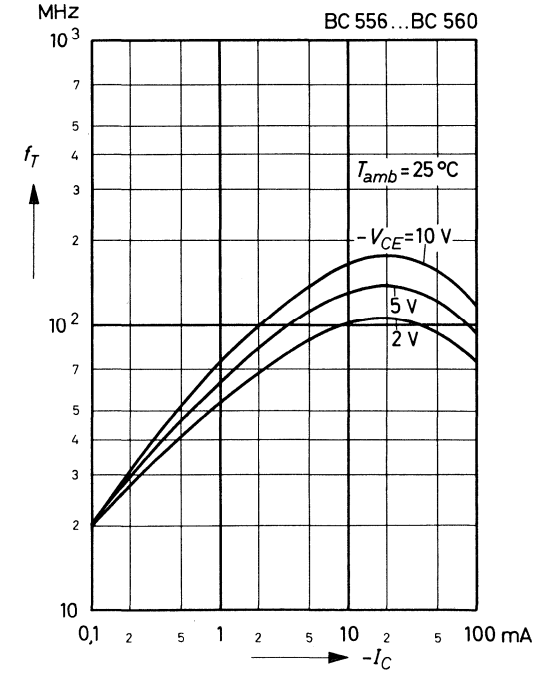
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



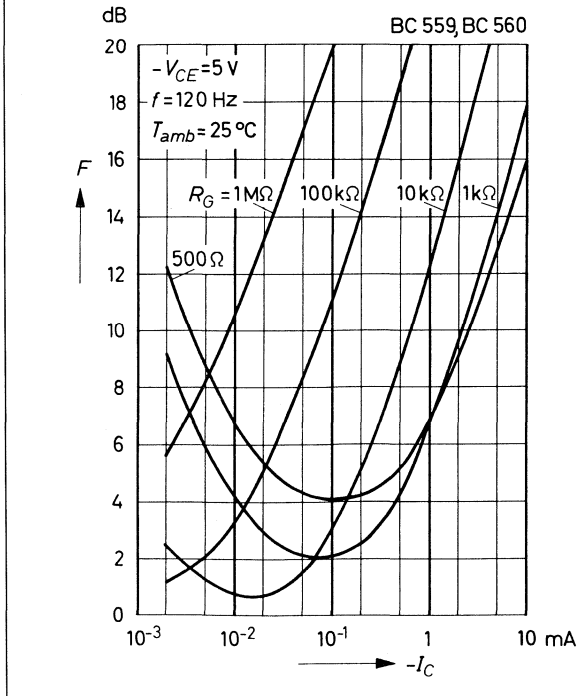
Relative h-parameters versus collector current



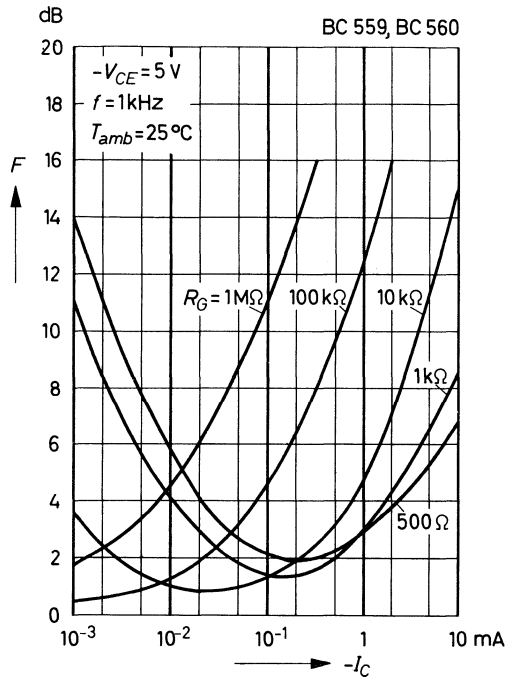
Gain bandwidth product versus collector current



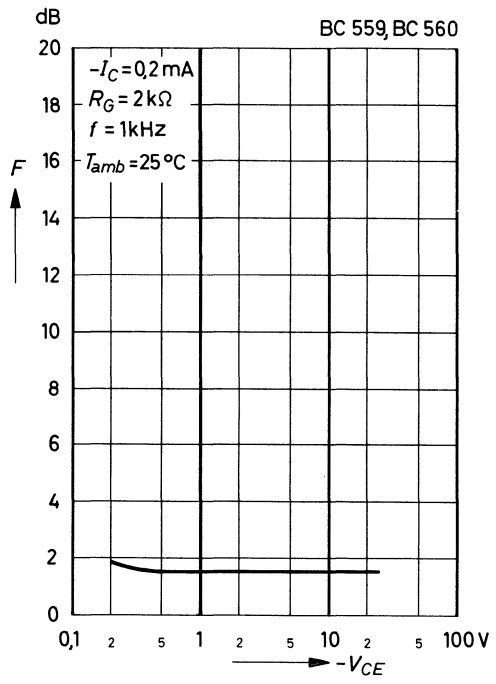
Noise figure versus collector current



Noise figure
versus collector current



Noise figure
versus collector emitter voltage

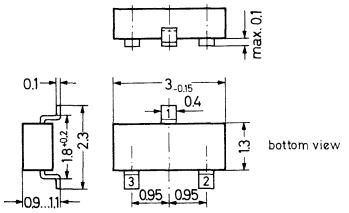


BC807, BC808

PNP Silicon Epitaxial Planar Transistors
for switching, AF driver and amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups -16, -25 and -40 according to their current gain.
As complementary types the NPN transistors BC817 and BC818 are recommended.
The pinconfiguration of these types is the following: 1 = Collector, 2 = Base, 3 = Emitter.



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Marking code

Type	Marking
BC807-16	5A
-25	5B
-40	5C
BC808-16	5E
-25	5F
-40	5G

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BC807**	$-V_{CES}$	50	V
	BC808	$-V_{CES}$	30	V
Collector Emitter Voltage	**BC807**	$-V_{CEO}$	45	V
	BC808	$-V_{CEO}$	25	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	500	mA
Peak Collector Current		$-I_{CM}$	1000	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	1000	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 . . . +150	°C

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

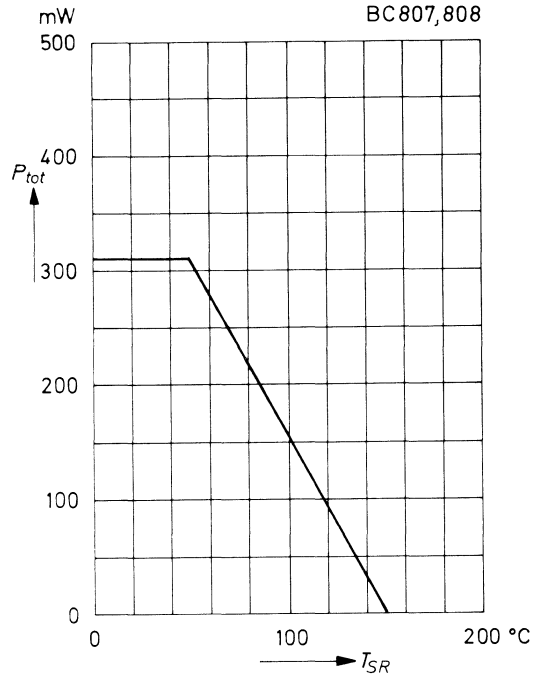
Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain						
at $-V_{CE}$ = 1 V, $-I_C$ = 100 mA	**Current Gain Group-16**	h_{FE}	100	–	250	–
	-25	h_{FE}	160	–	400	–
	-40	h_{FE}	250	–	600	–
at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA	**-16**	h_{FE}	60	–	–	–
	-25	h_{FE}	100	–	–	–
	-40	h_{FE}	170	–	–	–
Thermal Resistance Junction Substrate Backside		R_{thSB}	–	–	320[1)]	k/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage at $-I_C$ = 500 mA, $-I_B$ = 50 mA		$-V_{CEsat}$	–	–	0.7	V
Base Emitter Voltage at $-V_{CE}$ = 1 V, $-I_C$ = 300 mA		$-V_{BE}$	–	–	1.2	V
Collector Cutoff Current						
at $-V_{CE}$ = 45 V	**BC 807**	$-I_{CES}$	–	–	100	nA
at $-V_{CE}$ = 25 V	**BC 808**	$-I_{CES}$	–	–	100	nA
at $-V_{CE}$ = 25 V, T_j = 150 °C		$-I_{CES}$	–	–	5	μA
Emitter Cutoff Current at $-V_{EB}$ = 4 V		$-I_{EBO}$	–	–	100	nA
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz		f_T	–	100	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz		C_{CBO}		12		pF

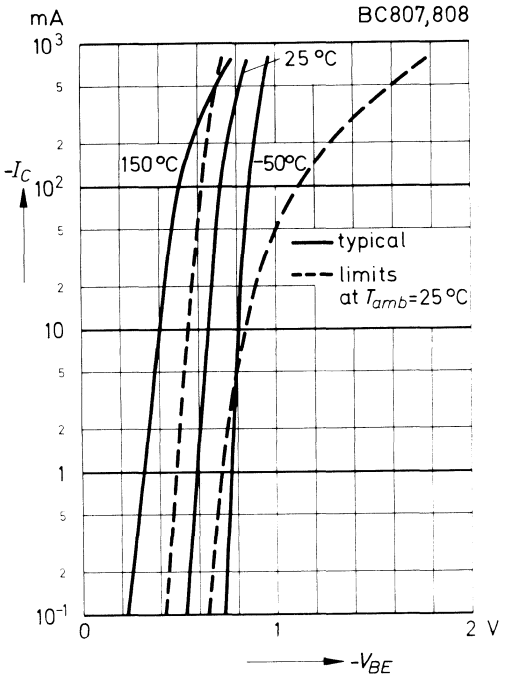
[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Admissible power dissipation versus temperature of substrate backside

Ceramic Substrate 0.7 mm; 2.5 cm² area.

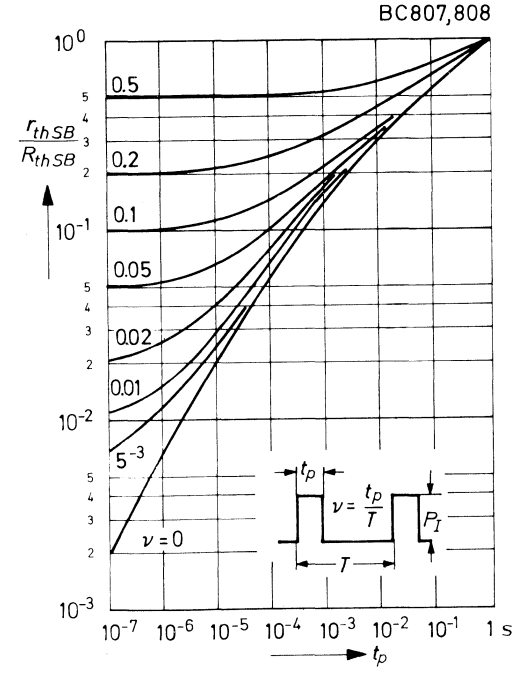


Collector current versus base emitter voltage

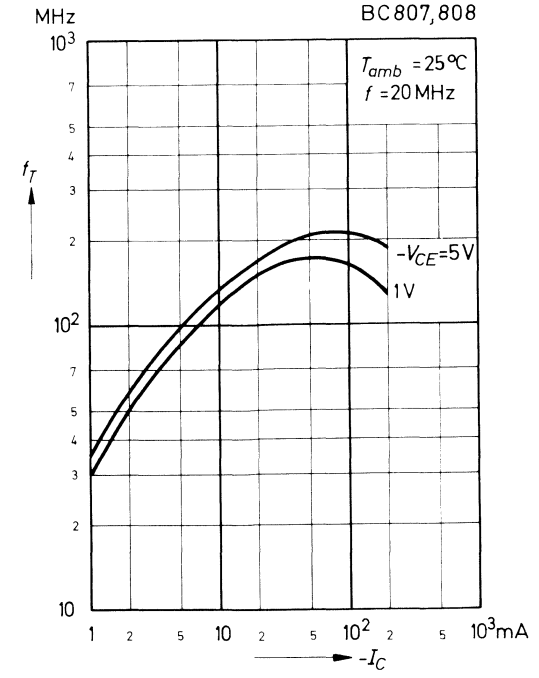


Pulse thermal resistance versus pulse duration (normalized)

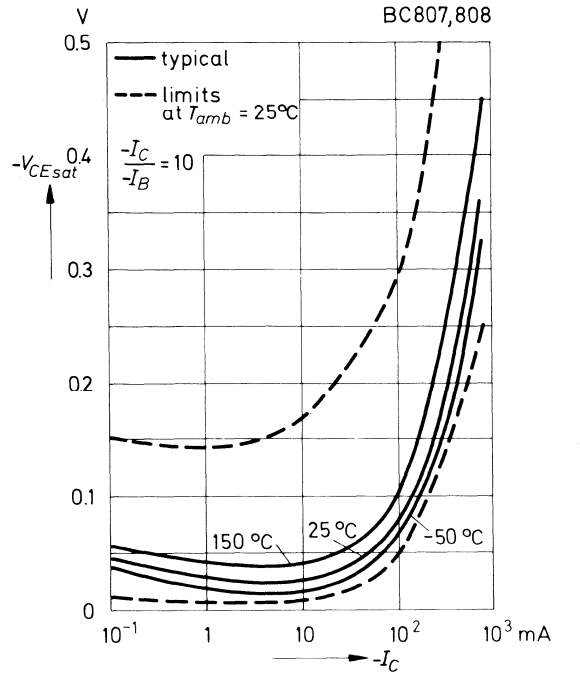
Ceramic Substrate 0.7 mm; 2.5 cm² area.



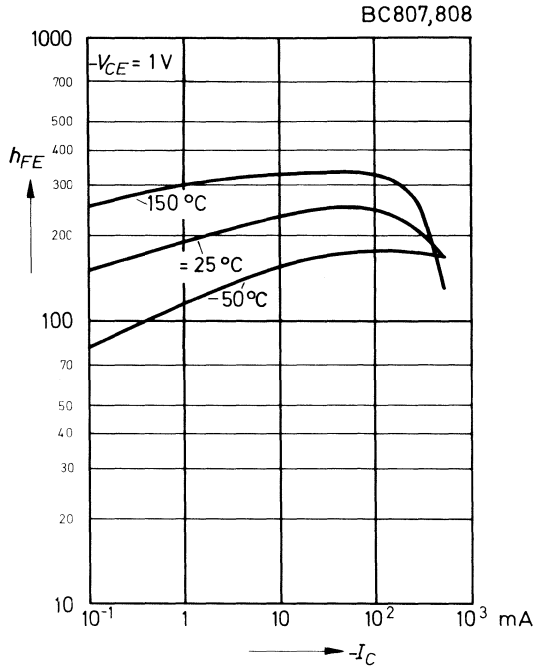
Gain bandwidth product versus collector current



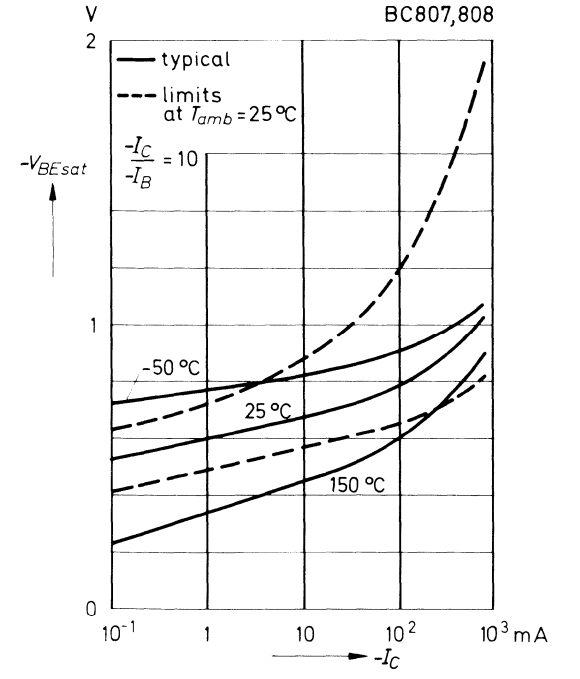
Collector saturation voltage versus collector current



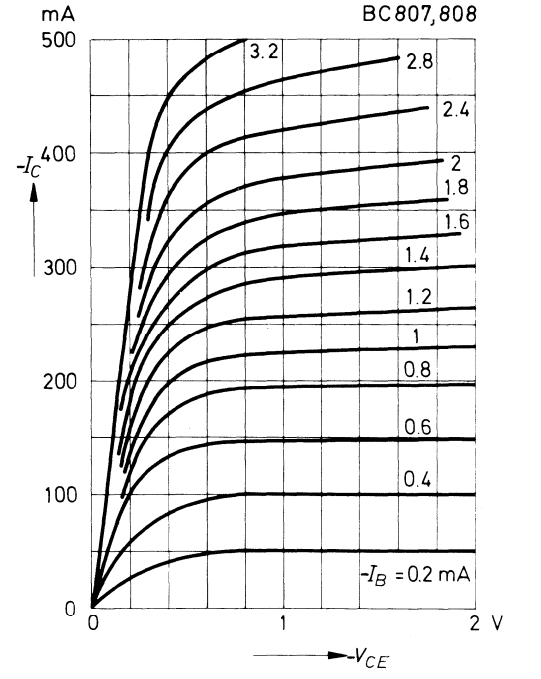
DC current gain versus collector current



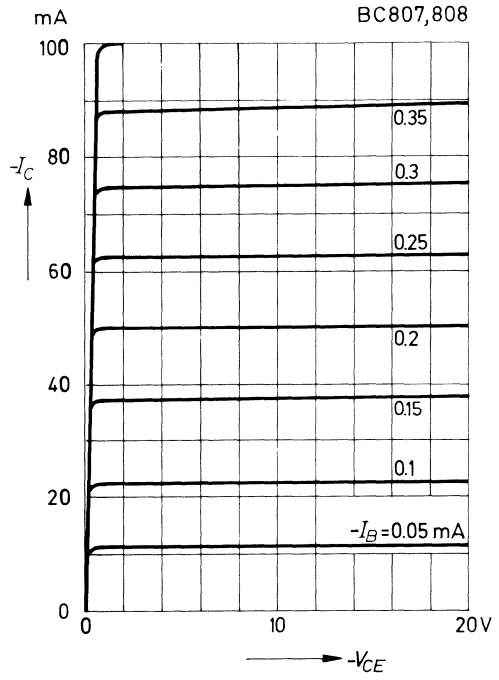
Base saturation voltage versus collector current



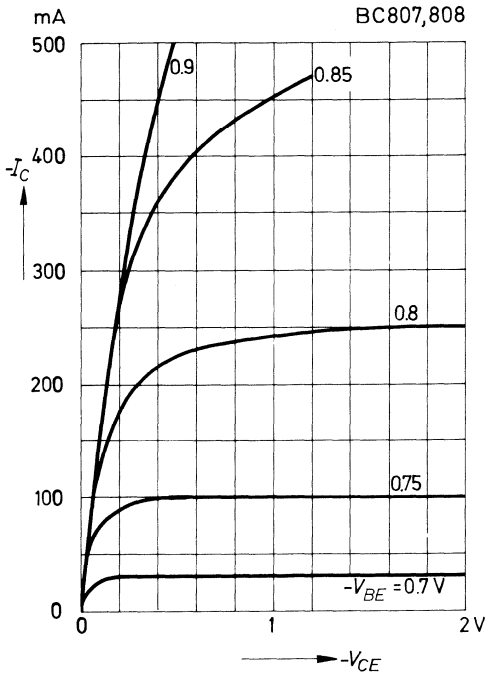
Common emitter collector characteristics



Common emitter collector characteristics



Common emitter collector characteristics

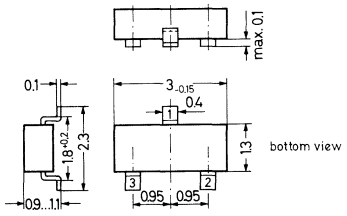


BC856 ... BC860

PNP Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors are subdivided into three groups A, B and C according to their current gain. BC856 is available in groups A and B, however, the types BC857, BC858, BC859 and BC860 can be supplied in all three groups. The BC859 is a low noise type and the BC860 a extremely low noise type. As complementary types the NPN transistors BC846 ... BC850 are recommended.
The pinconfiguration of these types is the following: 1 = Collector, 2 = Base, 3 = Emitter.



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Marking code

Type	Marking
BC856A	3A
B	3B
BC857A	3E
B	3F
C	3G
BC858A	3J
B	3K
C	3L

Marking code

Type	Marking
BC859A	4A
B	4B
C	4C
BC860A	4E
B	4F
C	4G

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC856**	$-V_{CBO}$	80	V
	BC857, BC860	$-V_{CBO}$	50	V
	BC858, BC859	$-V_{CBO}$	30	V
Collector Emitter Voltage	**BC856**	$-V_{CES}$	80	V
	BC857, BC860	$-V_{CES}$	50	V
	BC858, BC859	$-V_{CES}$	30	V
Collector Emitter Voltage	**BC856**	$-V_{CEO}$	65	V
	BC857, BC860	$-V_{CEO}$	45	V
	BC858, BC859	$-V_{CEO}$	30	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Peak Collector Current		$-I_{CM}$	200	mA
Peak Base Current		$-I_{BM}$	200	mA
Peak Emitter Current		I_{EM}	200	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 ... +150	°C

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz						
Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio	**Current Gain Group A**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at $-V_{CE}$ = 5 V, $-I_C$ = 10 μA	**Current Gain Group A**	h_{FE}	–	90	–	–
	B	h_{FE}	–	150	–	–
	C	h_{FE}	–	270	–	–
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA	**Current Gain Group A**	h_{FE}	110	180	220	–
	B	h_{FE}	200	290	450	–
	C	h_{FE}	420	520	800	–
Thermal Resistance Junction Substrate Backside		R_{thSB}	–	–	320[1]	K/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA		$-V_{CEsat}$	–	90	300	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{CEsat}$	–	250	650	mV
Base Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA		$-V_{BEsat}$	–	700	–	mV
at $-I_C$ = 100 mA, $-I_B$ = 5 mA		$-V_{BEsat}$	–	900	–	mV
Base Emitter Voltage						
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA		$-V_{BE}$	600	660	750	mV
at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA		$-V_{BE}$	–	–	800	mV
Collector Cutoff Current						
at $-V_{CE}$ = 80 V	**BC846**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 50 V	**BC847, BC850**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 30 V	**BC848, BC849**	$-I_{CES}$	–	0.2	15	nA
at $-V_{CE}$ = 80 V, T_j = 125 °C	**BC846**	$-I_{CES}$	–	–	4	μA
at $-V_{CE}$ = 50 V, T_j = 125 °C	**BC847, BC850**	$-I_{CES}$	–	–	4	μA
at $-V_{CE}$ = 30 V, T_j = 125 °C	**BC848, BC849**	$-I_{CES}$	–	–	4	μA
at $-V_{CB}$ = 30 V		$-I_{CBO}$	–	–	15	nA
at $-V_{CB}$ = 30 V, T_j = 150 °C		$-I_{CBO}$	–	–	5	μA
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 100 MHz		f_T	–	150	–	MHz
Collector Base Capacitance at $-V_{CB}$ = 10 V, f = 1 MHz		C_{CBO}	–	–	6	pF
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f = 1 kHz, △f = 200Hz	**BC856, BC857, BC858**	F	–	2	10	dB
	BC859, BC860	F	–	1	4	dB

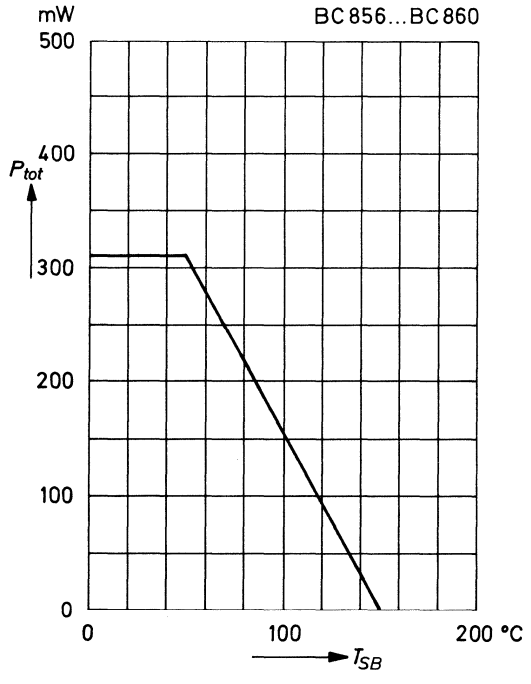
[1] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics, continuation

		Symbol	Min.	Typ.	Max.	Unit
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f = 30 . . . 15000 Hz	**BC859** **BC860**	F F	– –	1.2 1.2	4 2	dB dB
Equivalent Noise EMF at $-V_{CE}$ = 5 V, $-I_C$ = 200 μA, R_G = 2 kΩ, f = 10 . . . 50 Hz	**BC860**	v_r	–	–	0.11	μV

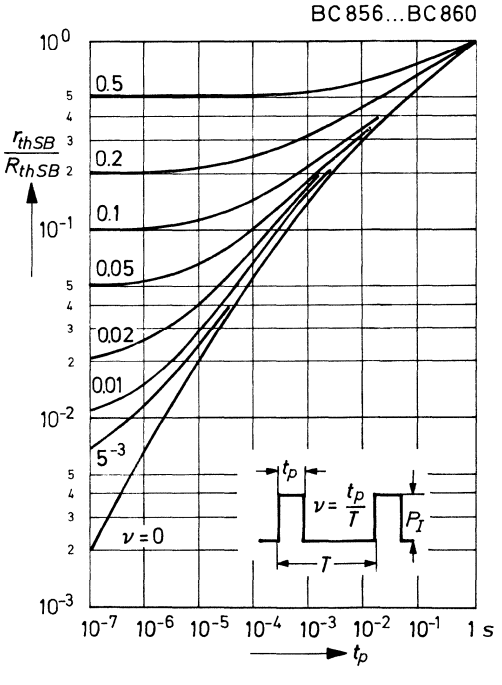
Admissible power dissipation versus temperature of substrate backside

Ceramic substrate 0.7 mm; 2.5 cm² area.

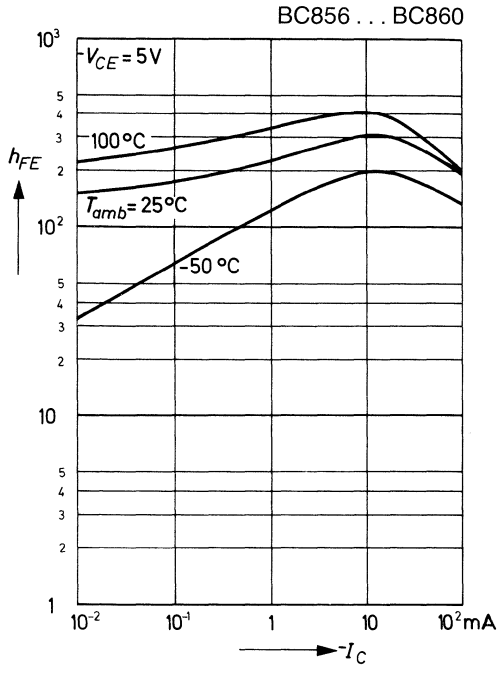


Pulse thermal resistance versus pulse duration (normalized)

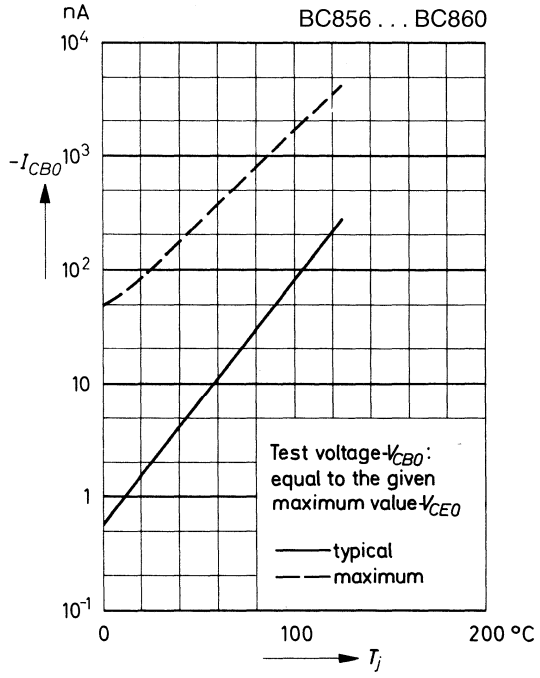
Ceramic substrate 0.7 mm; 2.5 cm² area.



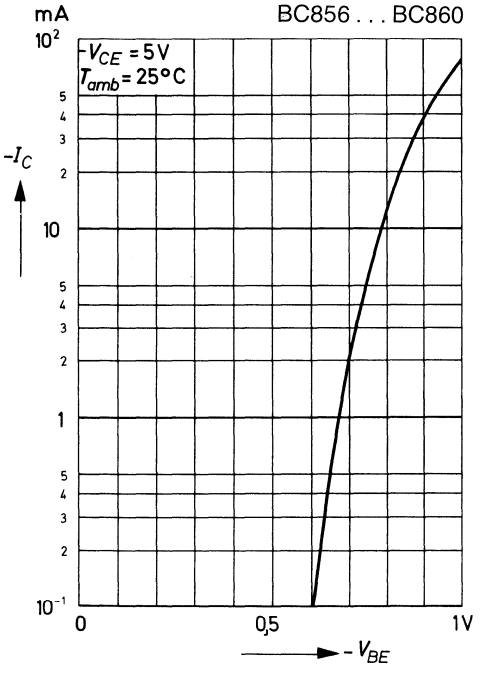
DC current gain versus collector current



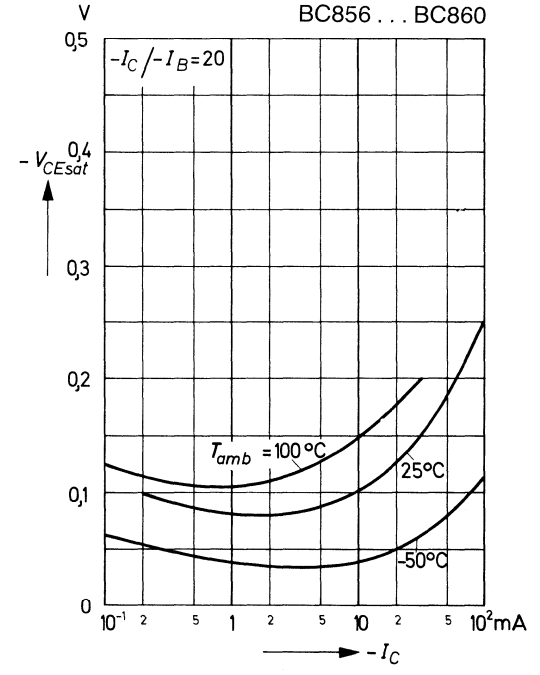
Collector cutoff current versus junction temperature



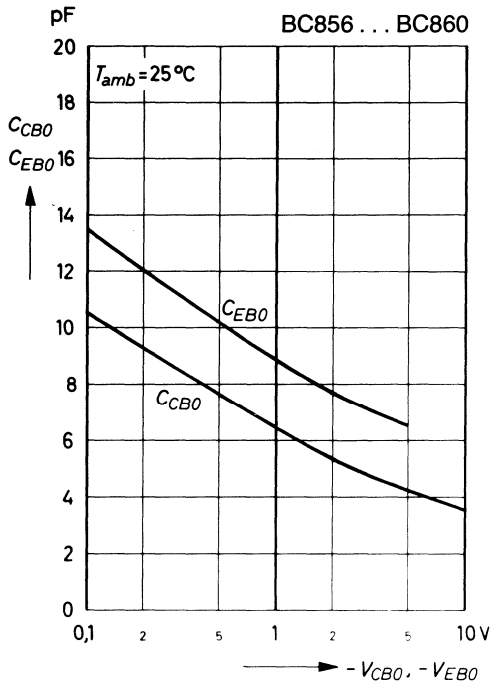
Collector current versus base emitter voltage



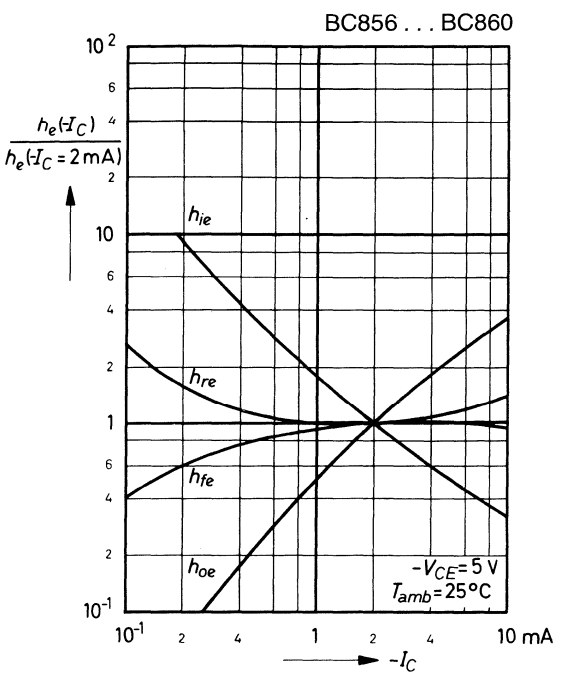
Collector saturation voltage versus collector current



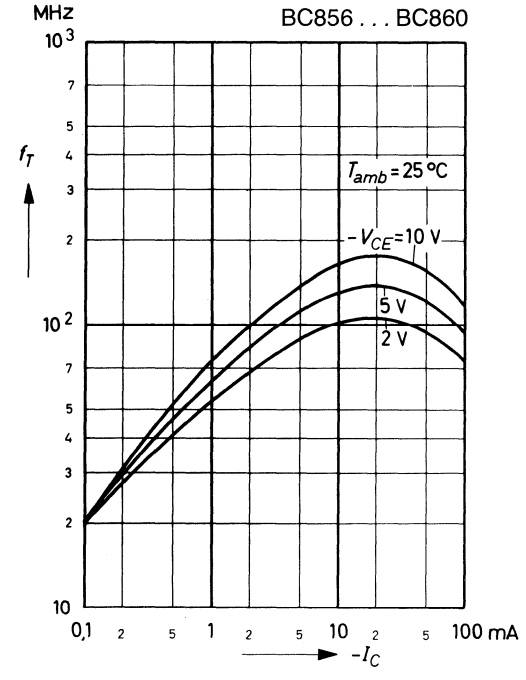
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



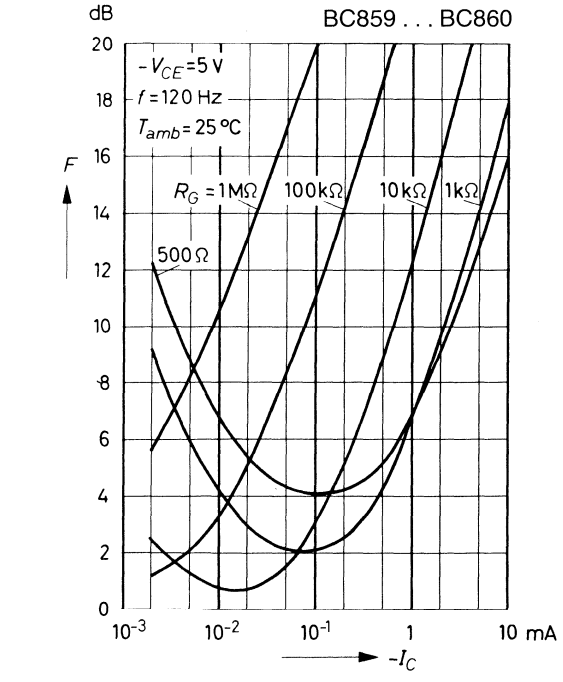
Relative h-parameters versus collector current



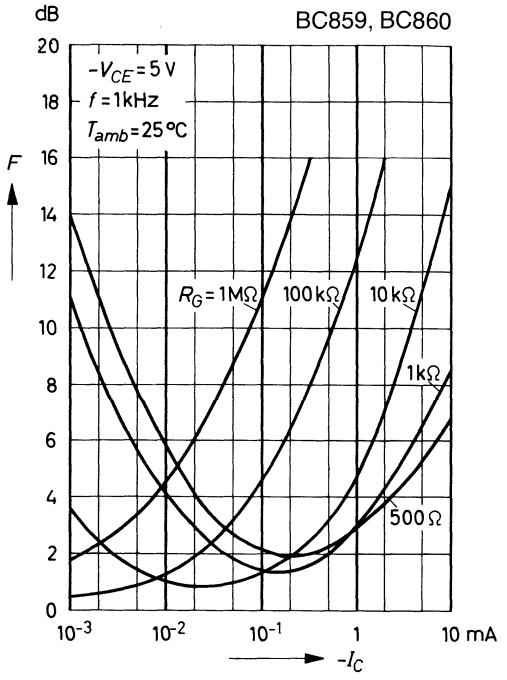
Gain bandwidth product versus collector current



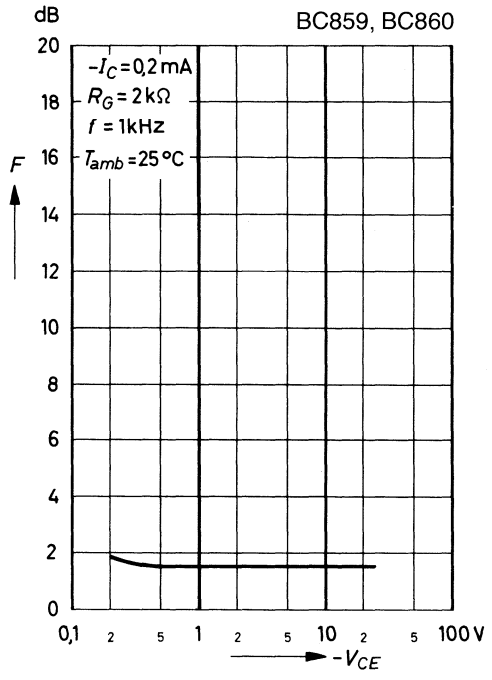
Noise figure versus collector current



Noise figure
versus collector current



Noise figure
versus collector emitter voltage

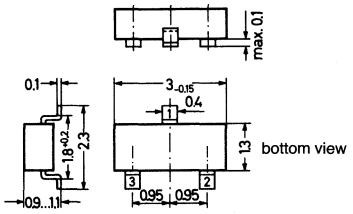


BCW61, BCX71

PNP Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

Especially suited for automatic insertion in thick- and thin-film circuits.

These transistors BCW61 are subdivided into the groups A, B, C and D, the transistors BCX71 into the groups G, H, J and K according to their current gain. As complementary types the NPN transistors BCW60 and BCX70 are recommended.
The pinconfiguration of these types is the following: 1 = Collector, 2 = Base, 3 = Emitter.



Plastic package 23A3
according to DIN 41869 (≈ TO-236)
The case is impervious to light

Weight approximately 0.01 g
Dimensions in mm

Marking code

Type	Marking
BCW61A	BA
BCW61B	BB
BCW61C	BC
BCW61D	BD

Marking code

Type	Marking
BCX71G	BG
BCX71H	BH
BCX71J	BJ
BCX71K	BK

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**BCW61**	$-V_{CES}$	32	V
	BCX71	$-V_{CES}$	45	V
Collector Emitter Voltage	**BCW61**	$-V_{CEO}$	32	V
	BCX71	$-V_{CEO}$	45	V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	200	mA
Base Current		$-I_B$	50	mA
Power Dissipation at T_{SB} = 50 °C		P_{tot}	310[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 to +150	°C

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA, f = 1 kHz						
Current Gain	**Group A, G**	h_{fe}	–	200	–	–
	B, H	h_{fe}	–	260	–	–
	C, J	h_{fe}	–	330	–	–
	D, K	h_{fe}	–	520	–	–
Input Impedance	**Group A, G**	h_{ie}	1.6	2.7	4.5	kΩ
	B, H	h_{ie}	2.5	3.6	6	kΩ
	C, J	h_{ie}	3.2	4.5	8.5	kΩ
	D, K	h_{ie}	4.5	7.5	12	kΩ
Output Admittance	**Group A, G**	h_{oe}	–	18	30	μS
	B, H	h_{oe}	–	24	50	μS
	C, J	h_{oe}	–	30	60	μS
	D, K	h_{oe}	–	50	100	μS
Reverse Voltage Transfer Ratio	**Group A, G**	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B, H	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C, J	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	D, K	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at $-V_{CE}$ = 5 V, $-I_C$ = 10 μA	**Group A, G**	h_{FE}	–	140	–	–
	B, H	h_{FE}	30	200	–	–
	C, J	h_{FE}	40	270	–	–
	D, K	h_{FE}	100	340	–	–
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA	**Group A, G**	h_{FE}	120	170	220	–
	B, H	h_{FE}	180	250	310	–
	C, J	h_{FE}	250	350	460	–
	D, K	h_{FE}	380	500	630	–
at $-V_{CE}$ = 1 V, $-I_C$ = 50 mA	**Group A, G**	h_{FE}	60	–	–	–
	B, H	h_{FE}	80	–	–	–
	C, J	h_{FE}	100	–	–	–
	D, K	h_{FE}	110	–	–	–
Thermal Resistance Junction to Substrate Backside		R_{thSB}	–	–	320[1)]	K/W
Thermal Resistance Junction to Ambient		R_{thA}	–	–	450	K/W
Collector Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.25 mA		$-V_{CEsat}$	–	120	250	mV
at $-I_C$ = 50 mA, $-I_B$ = 1.25 mA		$-V_{CEsat}$	–	250	500	mV
Base Saturation Voltage						
at $-I_C$ = 10 mA, $-I_B$ = 0.25 mA		$-V_{BEsat}$	–	700	850	mV
at $-I_C$ = 50 mA, $-I_B$ = 1.25 mA		$-V_{BEsat}$	–	800	1050	mV
Base Emitter Voltage						
at $-V_{CE}$ = 5 V, $-I_C$ = 10 μA		$-V_{BE}$	–	550	–	mV
at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA		$-V_{BE}$	600	650	750	mV
at $-V_{CE}$ = 1 V, $-I_C$ = 50 mA		$-V_{BE}$	–	720	–	mV
Collector Cutoff Current						
at $-V_{CE}$ = 32 V	**BCW61**	$-I_{CES}$	–	–	20	nA
at $-V_{CE}$ = 32 V, T_{amb} = 150 °C		$-I_{CES}$	–	–	20	μA
at $-V_{CE}$ = 45 V	**BCX71**	$-I_{CES}$	–	–	20	nA
at $-V_{CE}$ = 45 V, T_{amb} = 150 °C		$-I_{CES}$	–	–	20	μA
Emitter Cutoff Current		$-I_{EBO}$	–	–	20	nA
at $-V_{EB}$ = 4 V						
Collector Emitter Breakdown Voltage						
at $-I_C$ = 2 mA	**BCW61**	$-U_{(BR)CEO}$	32	–	–	V
	BCX71	$-U_{(BR)CEO}$	45	–	–	V

[1)] Ceramic Substrate 0.7 mm; 2.5 cm^2 area

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Emitter Base Breakdown Voltage at $-I_E = 1\ \mu A$	$-U_{(BR)EBO}$	5	–	–	V
Gain Bandwidth Product at $-V_{CE} = 5$ V, $-I_C = 10$ mA, f = 100 MHz	f_T	–	180	–	MHz
Collector Base Capacitance at $-V_{CB} = 10$ V, f = 1 MHz	C_{CBO}	–	–	6	pF
Emitter Base Capacitance at $-V_{EB} = 0.5$ V, f = 1 MHz	C_{EBO}	–	11	–	pF
Noise Figure at $-V_{CE} = 5$ V, $-I_C = 200\ \mu A$, $R_G = 2\ k\Omega$, f = 1 kHz, $\triangle f = 200$ Hz	F	–	2	6	dB
Switching Times (see Fig. 1) at $-I_C = 10$ mA, $-I_{B1} = I_{B2} = 1$ mA					
Delay Time	t_d	–	35	–	ns
Rise Time	t_r	–	50	–	ns
Turn-On Time	$t_d + t_r$	–	85	150	ns
Storage Time	t_s	–	400	–	ns
Fall Time	t_f	–	80	–	ns
Turn-Off Time	$t_s + t_f$	–	480	800	ns

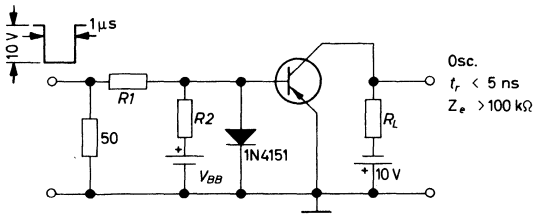
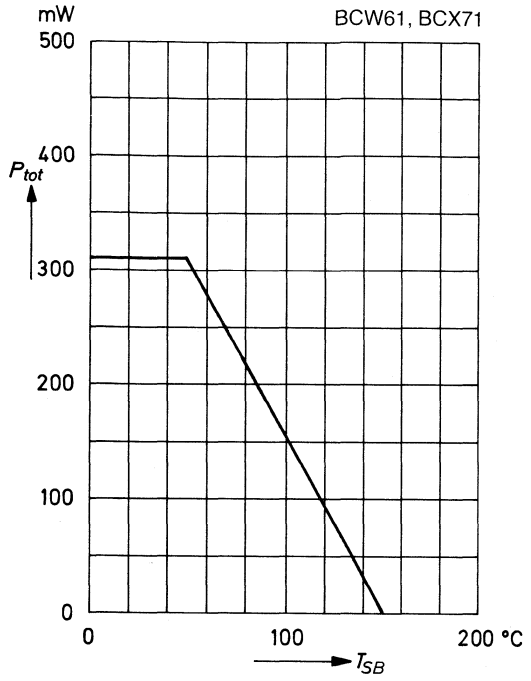


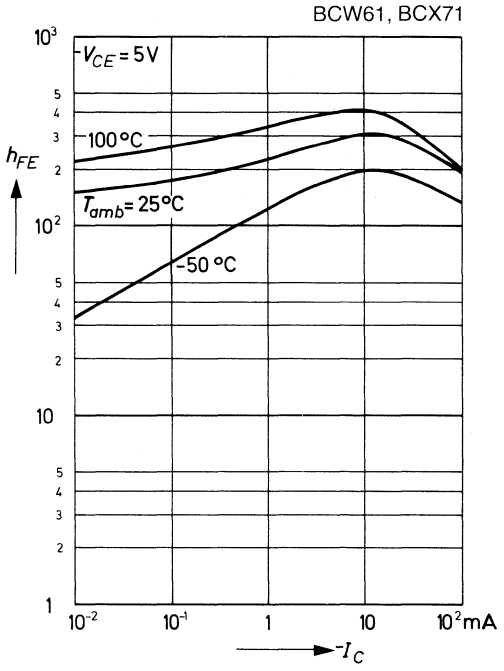
Fig. 1:
Test circuit for switching times

Admissible power dissipation versus temperature of substrate backside

Ceramic substrate 0.7 mm; 2.5 cm² area.

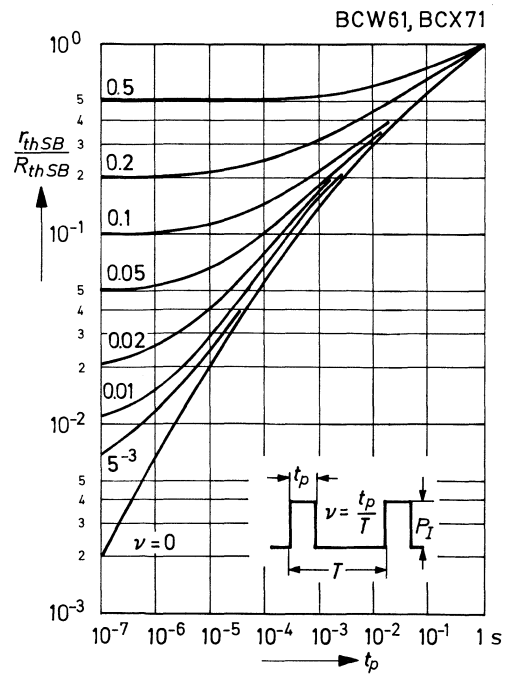


DC current gain versus collector current

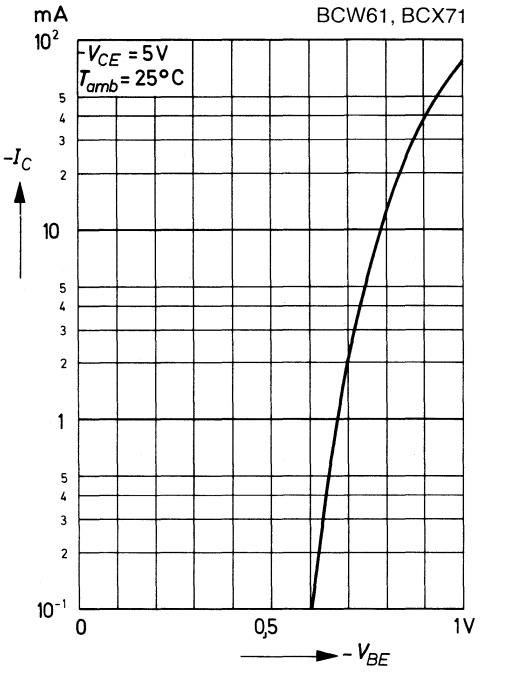


Pulse thermal resistance versus pulse duration (normalized)

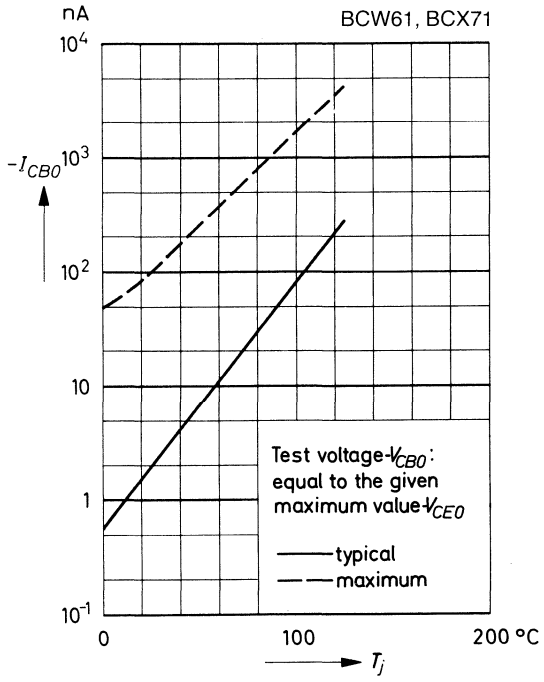
Ceramic Substrate 0.7 mm; 2.5 cm² area.



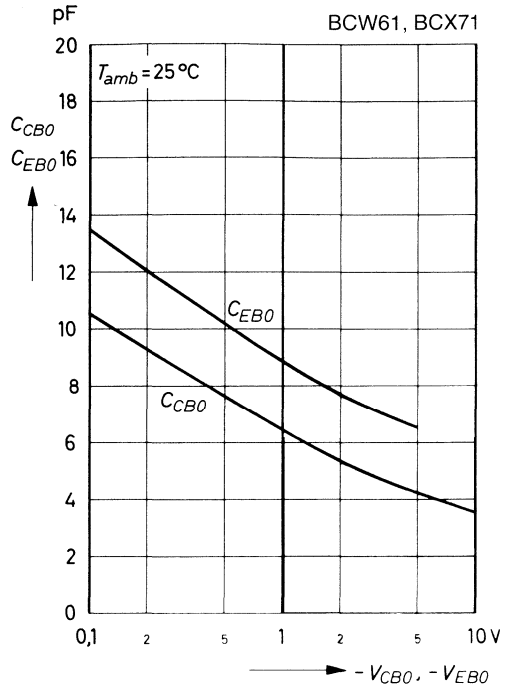
Collector current versus base emitter voltage



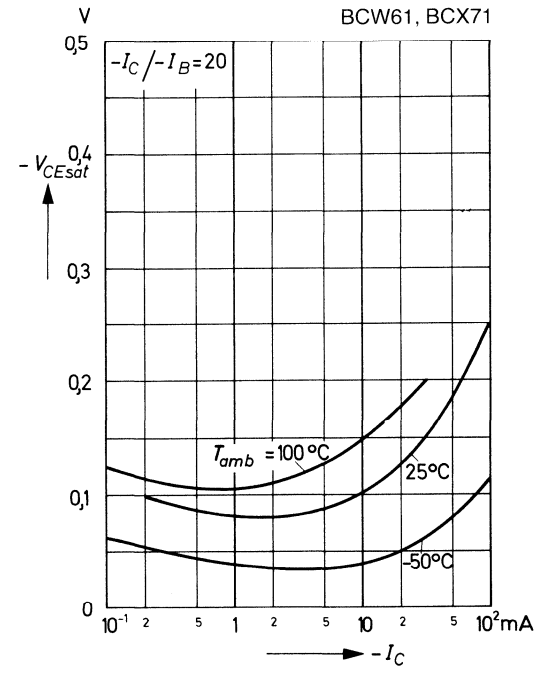
Collector cutoff current versus junction temperature



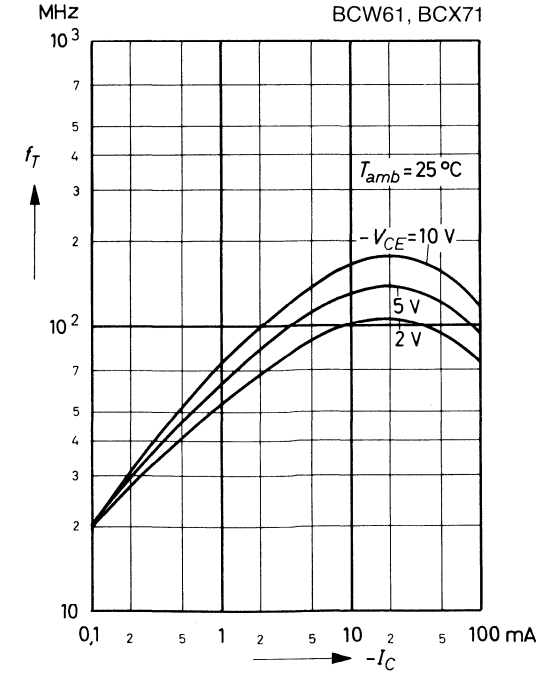
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



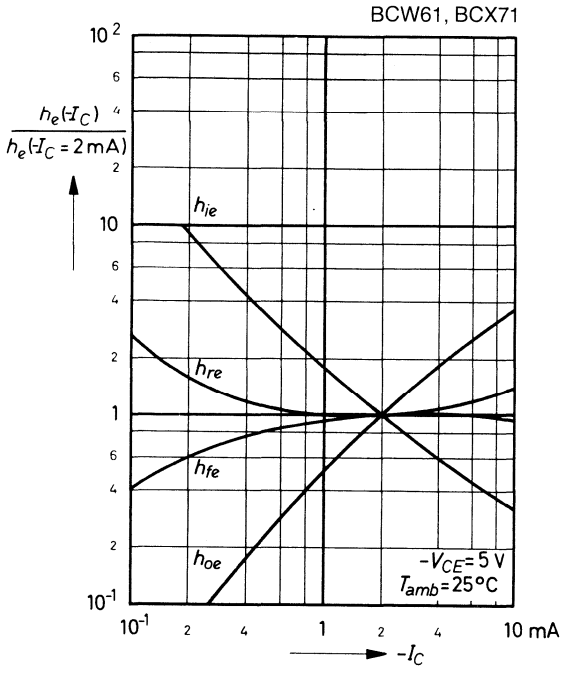
Collector saturation voltage versus collector current



Gain bandwidth product versus collector current



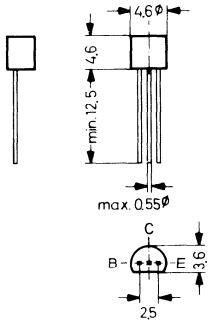
Relative h-parameters versus collector current



JA100, JA101

PNP Silicon Epitaxial Planar Transistors
for switching and amplifier applications

The transistors are subdivided into four groups O, P, Q and R according to their current gain.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Emitter Voltage	**JA101** **JA100**	$-V_{CES}$ $-V_{CES}$	50 30	V V
Collector Emitter Voltage	**JA101** **JA100**	$-V_{CEO}$ $-V_{CEO}$	45 25	V V
Emitter Base Voltage		$-V_{EBO}$	5	V
Collector Current		$-I_C$	100	mA
Peak Collector Current		$-I_{CM}$	200	mA
Base Current		$-I_B$	50	mA
Peak Base Current		$-I_{BM}$	100	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1)]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−55 . . . +150	°C

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

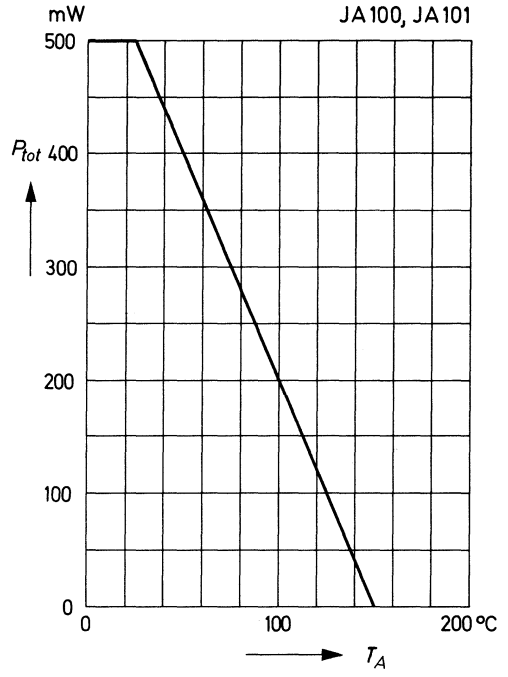
Characteristics at T_{amb} = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE}$ = 5 V, $-I_C$ = 1 mA **Current Gain Group O** **P** **Q** **R**	h_{FE} h_{FE} h_{FE} h_{FE}	90 135 200 300	– – – –	180 270 400 600	– – – –
Collector Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{CEsat}$ $-V_{CEsat}$	– –	0.08 0.25	0.3 0.65	V V
Base Saturation Voltage at $-I_C$ = 10 mA, $-I_B$ = 0.5 mA at $-I_C$ = 100 mA, $-I_B$ = 5 mA	$-V_{BEsat}$ $-V_{BEsat}$	– –	0.73 0.87	1.00 1.05	V V
Base Emitter Voltage at $-V_{CE}$ = 5 V, $-I_C$ = 0.1 mA at $-V_{CE}$ = 5 V, $-I_C$ = 2 mA at $-V_{CE}$ = 5 V, $-I_C$ = 100 mA	$-V_{BE}$ $-V_{BE}$ $-V_{BE}$	– 0.55 –	0.57 0.62 0.8	– 0.7 –	V V V
Collector Cutoff Current at $-V_{CE}$ = 45 V **JA101** at $-V_{CE}$ = 25 V **JA100** at $-V_{CE}$ = 45 V, T_j = 125 °C **JA101** at $-V_{CE}$ = 25 V, T_j = 125 °C **JA100**	 $-I_{CES}$ $-I_{CES}$ $-I_{CES}$ $-I_{CES}$	 – – – –	 2 2 – –	 15 15 4 4	 nA nA µA µA
Collector Emitter Breakdown Voltage at $-I_{CES}$ = 10 µA **JA101** **JA100** at $-I_{CEO}$ = 2 mA **JA101** **JA100**	 $-V_{(BR)CES}$ $-V_{(BR)CES}$ $-V_{(BR)CEO}$ $-V_{(BR)CEO}$	 50 30 45 25	 – – – –	 – – – –	 V V V V
Emitter Base Breakdown Voltage at $-I_{EBO}$ = 10 µA	$-V_{(BR)EBO}$	5	–	–	V
Gain Bandwidth Product at $-V_{CE}$ = 5 V, $-I_C$ = 10 mA, f = 50 MHz	f_T	–	130	–	MHz
Collector Base Capacitance at $-V_{CBO}$ = 10 V, f = 1 MHz	C_{CBO}	–	–	6	pF
Emitter Base Capacitance at $-V_{EBO}$ = 0.5 V, f = 1 MHz	C_{EBO}	–	12	–	pF
Noise Figure at $-V_{CE}$ = 5 V, $-I_C$ = 0.2 mA, R_G = 2 kΩ, f = 1 kHz	F	–	–	10	dB
Thermal Resistance Junction to Ambient	R_{thA}	–	–	250[1)]	K/W

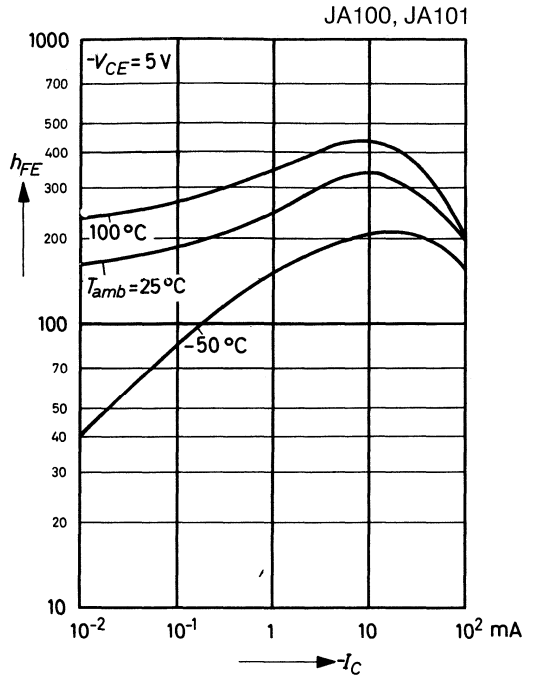
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Admissible power dissipation versus ambient temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.

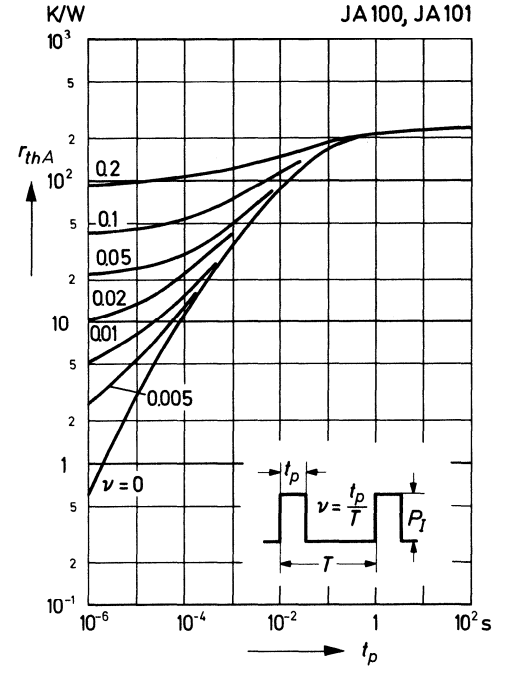


DC current gain versus collector current

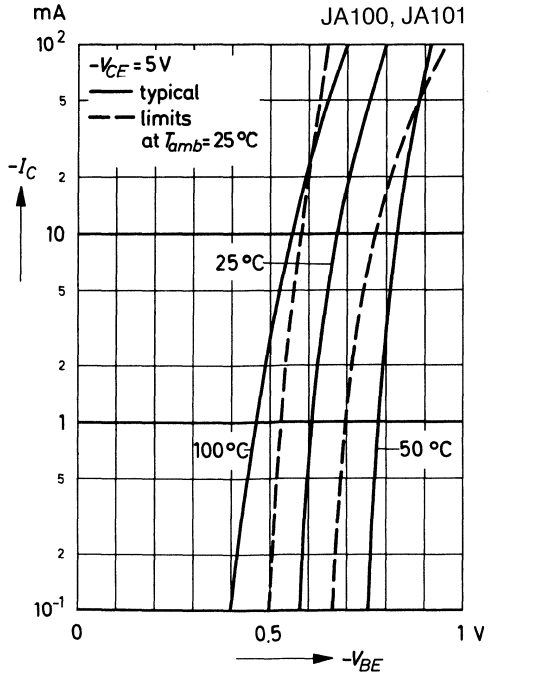


Pulse thermal resistance versus pulse duration

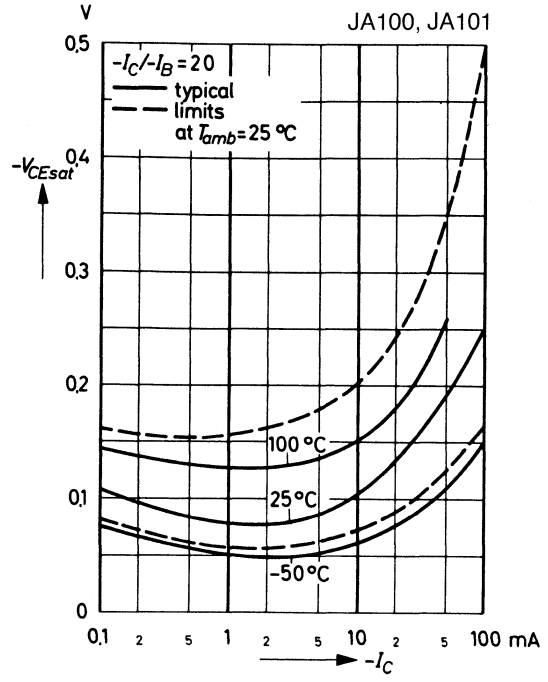
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



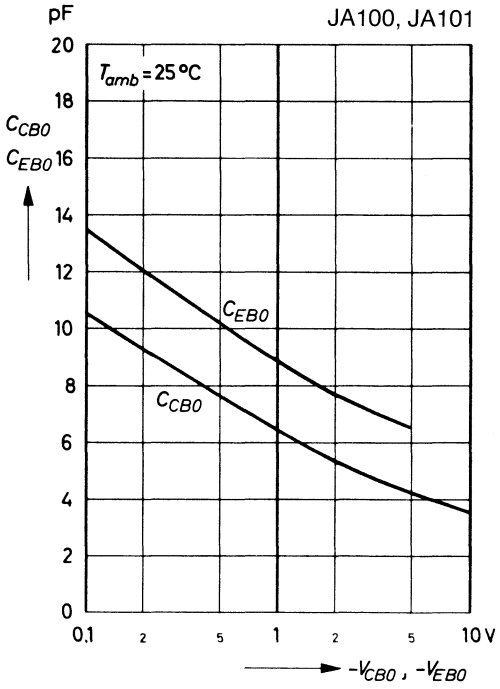
Collector current versus base emitter voltage



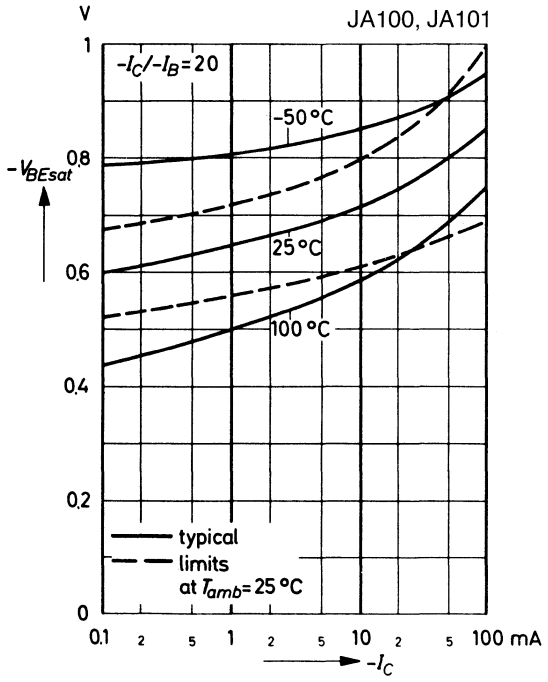
Collector saturation voltage versus collector current



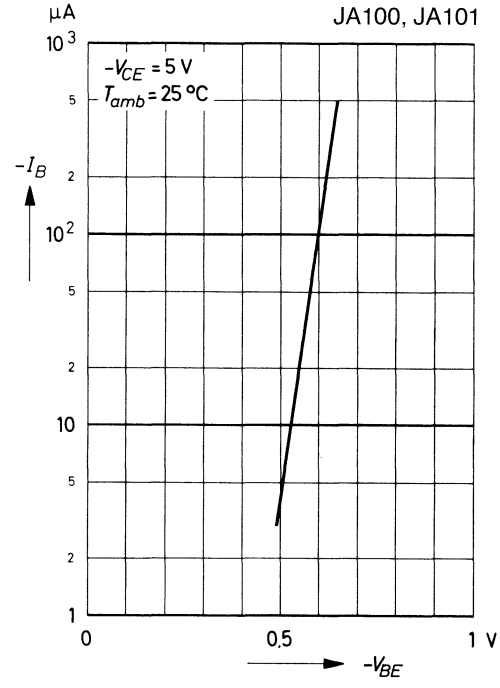
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



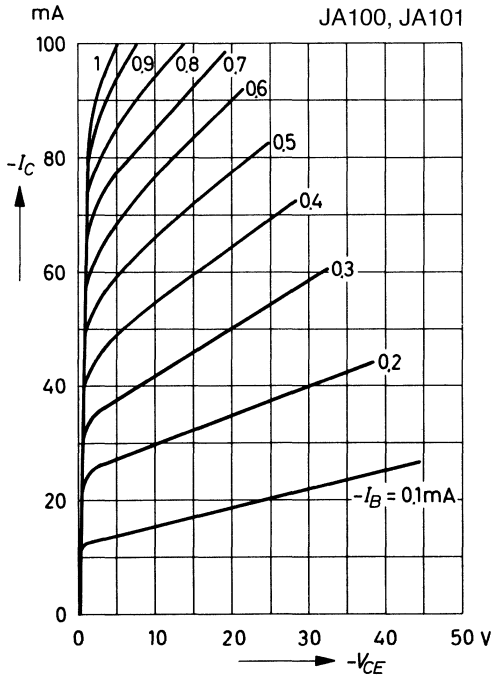
Base saturation voltage versus collector current



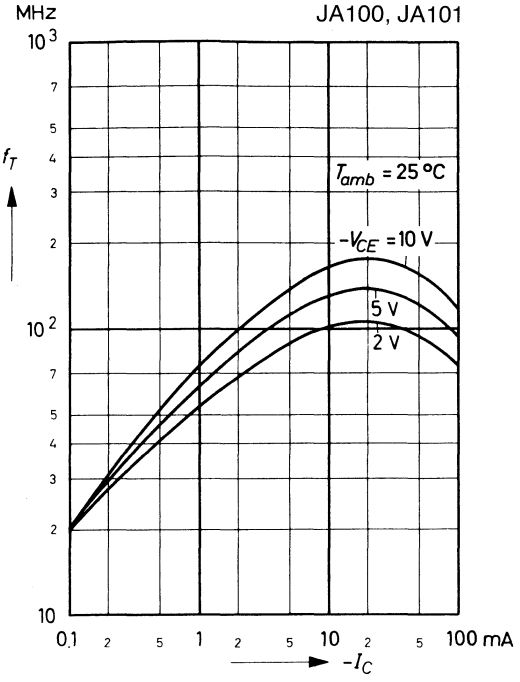
Common emitter input characteristic



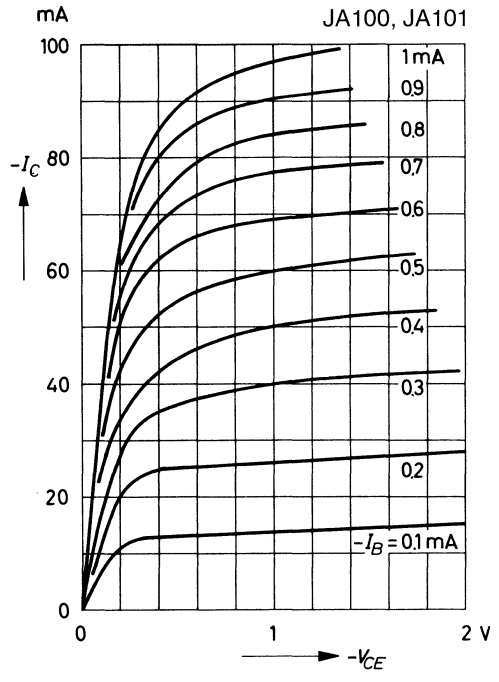
Common emitter collector characteristics



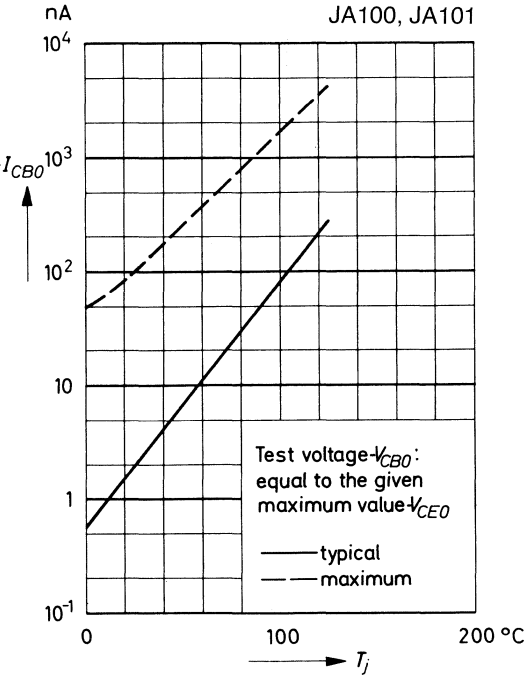
Gain bandwidth product versus collector emitter voltage



Common emitter collector characteristics



Collector cutoff current versus ambient temperature



VMOS Transistors

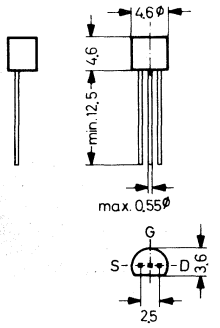
BS107

N-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	200	V
Drain Gate Voltage	V_{DGS}	200	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	120	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.5	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.5 A, T_j = 25 °C	V_F	0.85	V

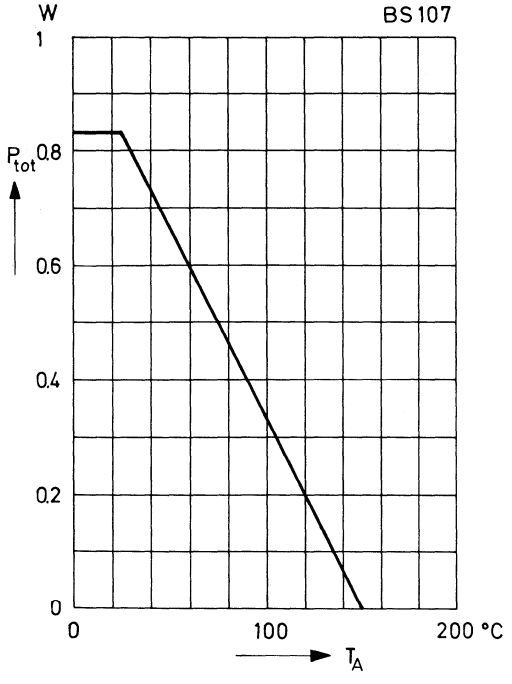
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu A$, $V_{GS} = 0$	$V_{(BR)DSS}$	200	230	–	V
Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$	I_{GSS}	–	–	10	nA
Drain Cutoff Current at $V_{DS} = 130$ V, $V_{GS} = 0$ at $V_{DS} = 70$ V, $V_{GS} = 0.2$ V	 I_{DSS} I_{DSX}	 – –	 – –	 30 1	 nA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS\,(TO)}$	–	1.8	3	V
Drain-Source ON Resistance at $V_{GS} = 2.8$ V, $I_D = 20$ mA	$r_{DS\,(ON)}$	–	18	28	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1]	K/W
Capacitances at $V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 58 8 1.5	 – – –	 pF pF pF
Switching Times at $V_{GS} = 10$ V, $V_{DS} = 10$ V, $R_D = 100\ \Omega$ Turn On Time Turn Of Time	 t_{on} t_{off}	 – –	 5 15	 – –	 ns ns

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

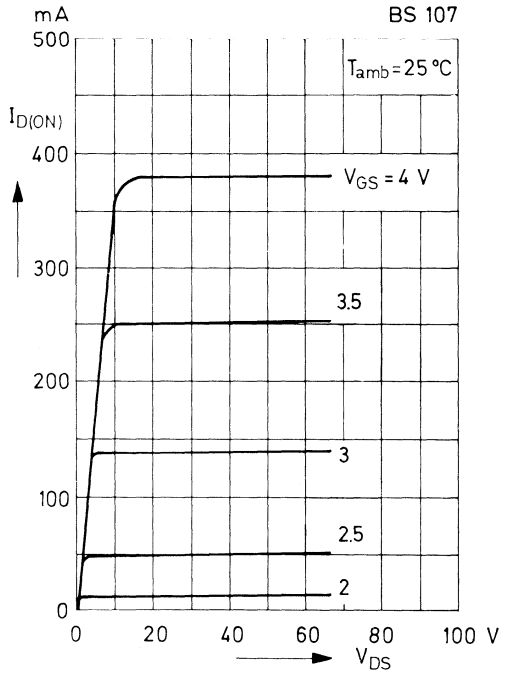
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



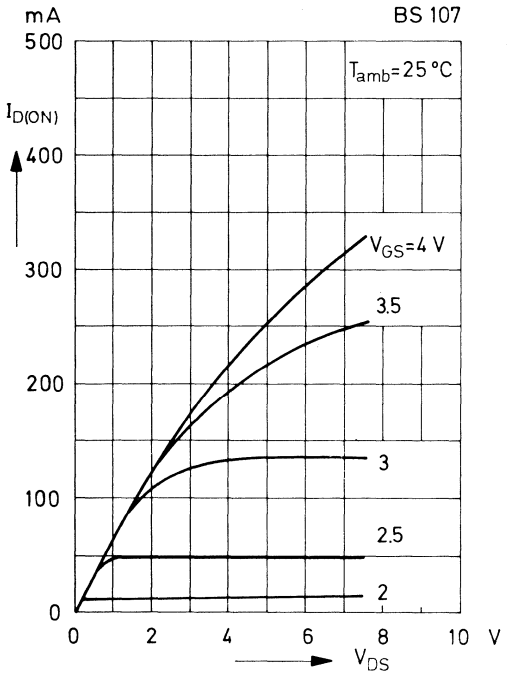
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%

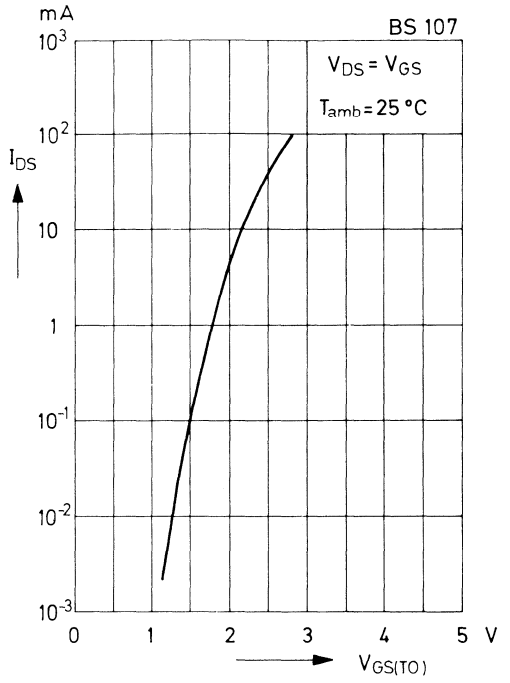


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%

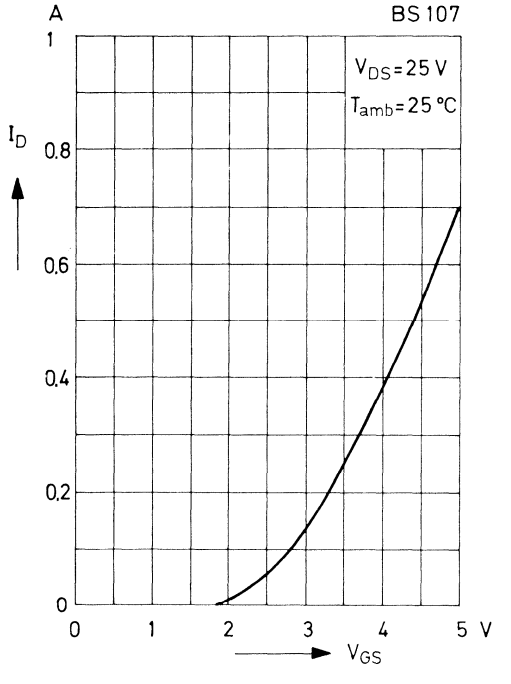


Drain-source current versus gate threshold voltage

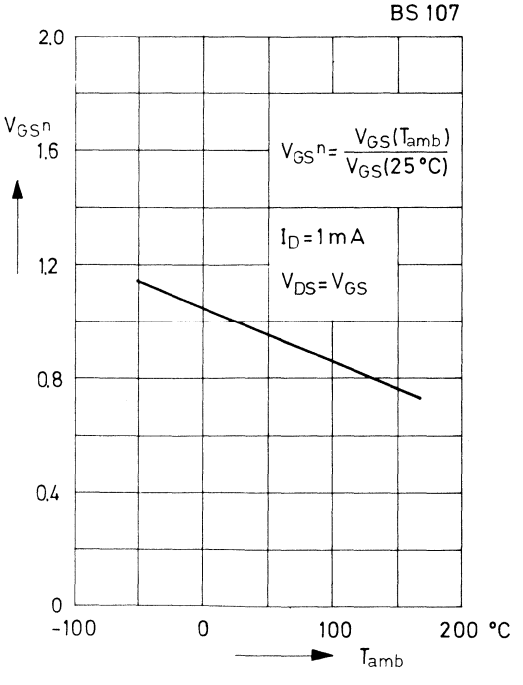


Drain current versus gate-source voltage

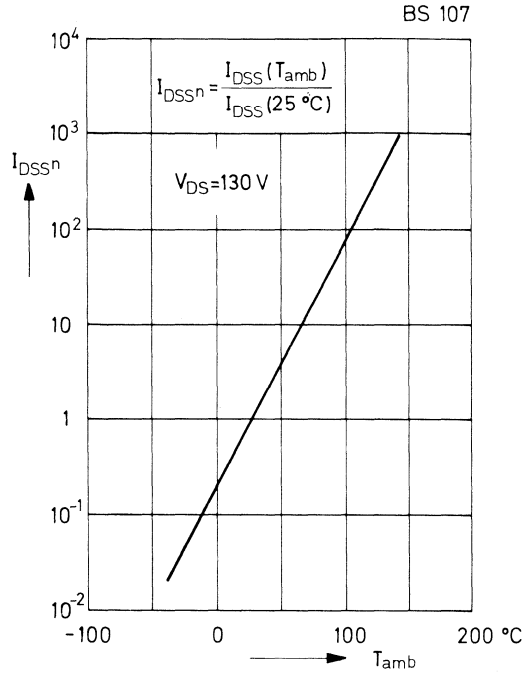
Pulse test width 80 μs; pulse duty factor 1%



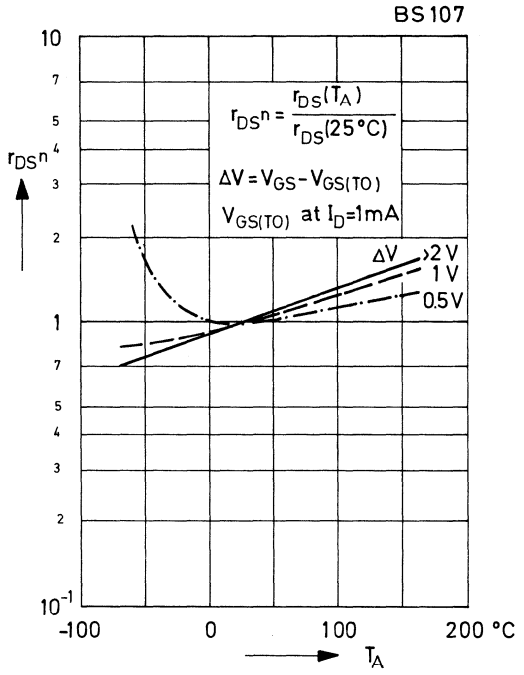
Normalized gate-source voltage versus temperature



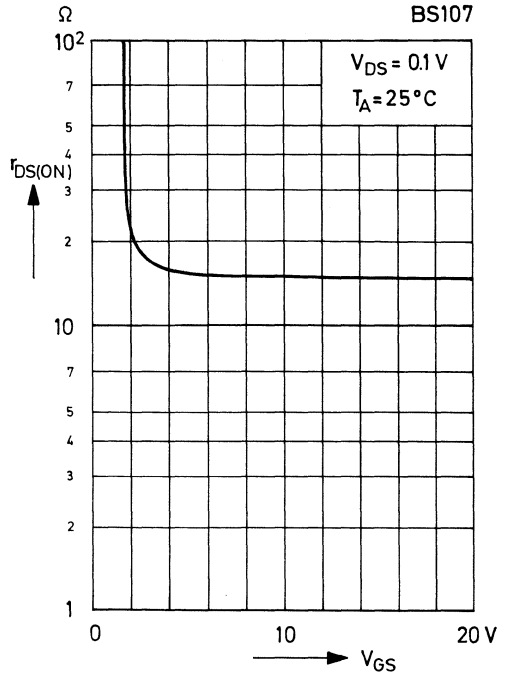
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

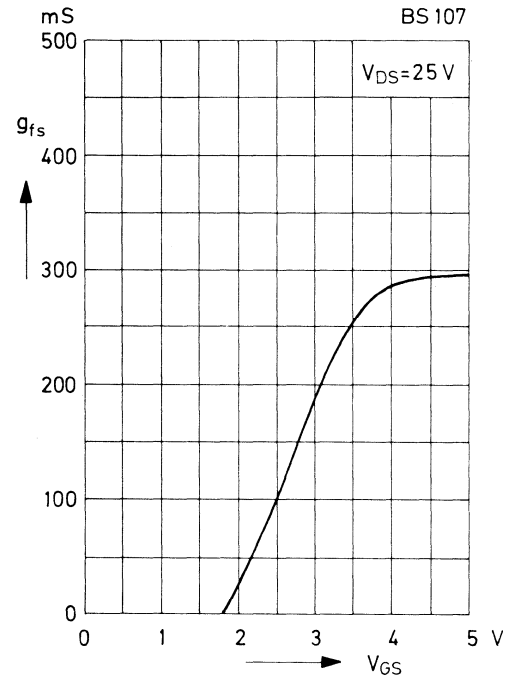


Drain-source resistance versus gate-source voltage



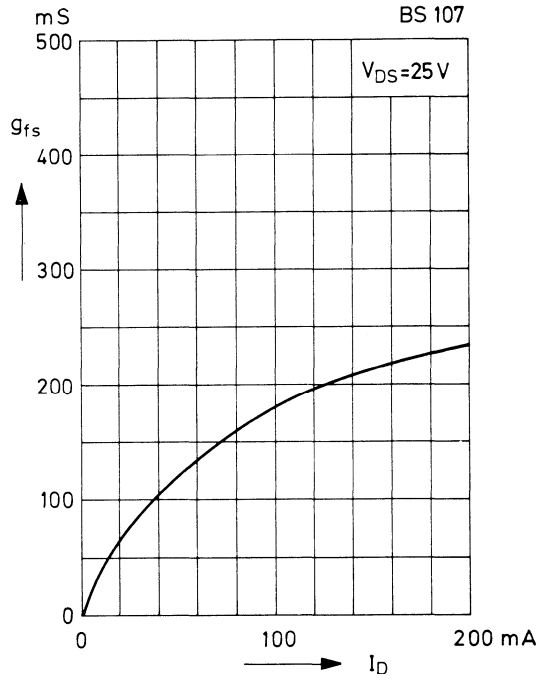
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%

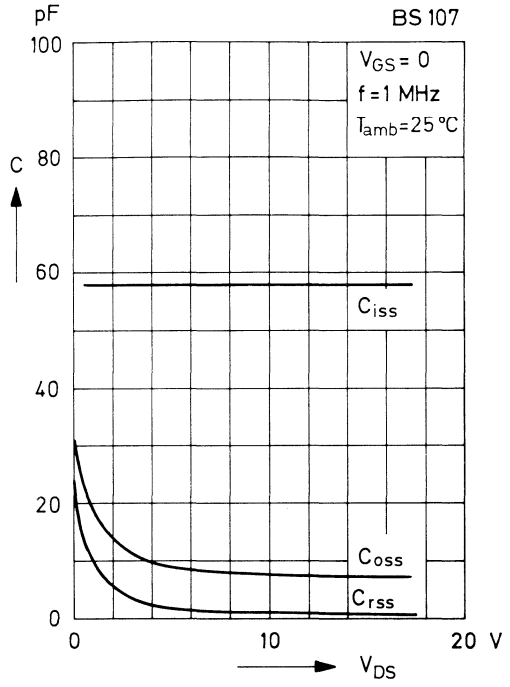


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%



Capacitance versus drain-source voltage



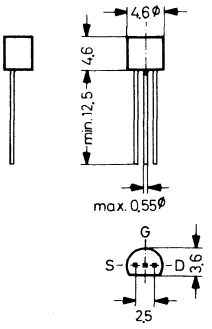
BS108

N-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source-Voltage	V_{DSS}	200	V
Drain-Gate-Voltage	V_{DGS}	200	V
Gate-Source-Voltage (pulsed)	V_{GS}	±20	V
Drain-Current (continuous)	I_D	230	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.75	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

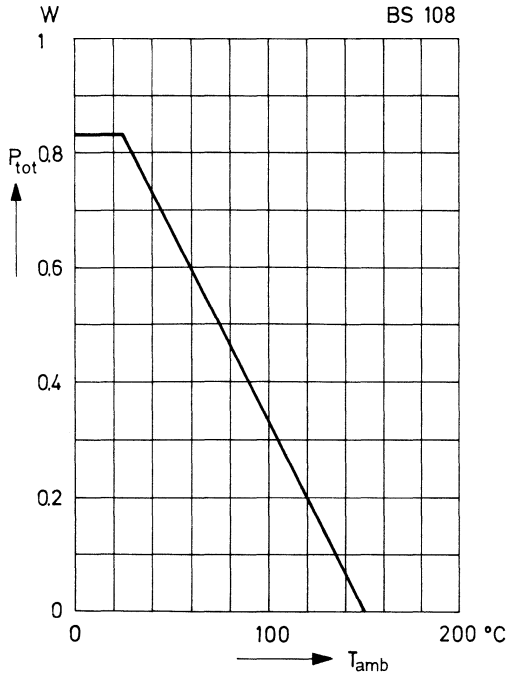
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu A$, $V_{GS} = 0$	$V_{(BR)DSS}$	200	230	–	V
Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$	I_{GSS}	–	–	10	nA
Drain Cutoff Current at $V_{DS} = 130$ V, $V_{GS} = 0$ at $V_{DS} = 70$ V, $V_{GS} = 0.2$ V	 I_{DSS} I_{DSX}	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS\,(TO)}$	–	1.5	2.5	V
Drain-Source ON Resistance at $V_{GS} = 2.8$ V, $I_D = 100$ mA	$r_{DS\,(ON)}$	–	5.5	8	Ω
Thermal Resistance Chip to open Air	R_{thA}	–	–	150[1)]	K/W
Capacitances at $V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 220 20 5	 – – –	 pF pF pF
Switching Times at $V_{GS} = 10$ V, $V_{DS} = 10$ V, $R_D = 100\ \Omega$ Turn On Time Turn Off Time	 t_{on} t_{off}	 – –	 5 50	 – –	 ns ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

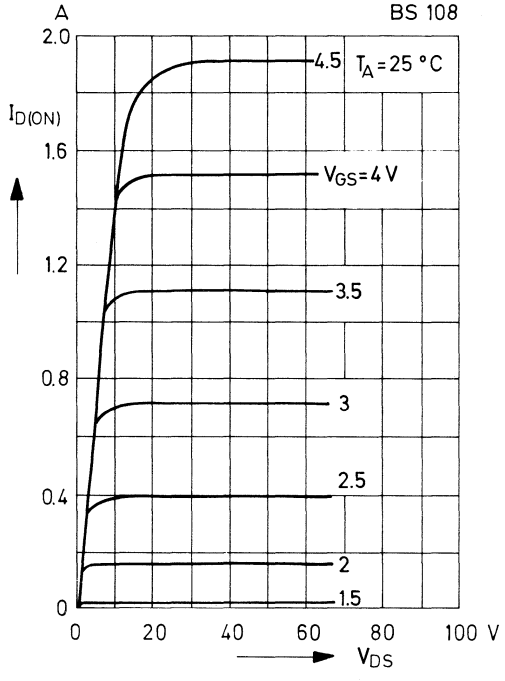
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



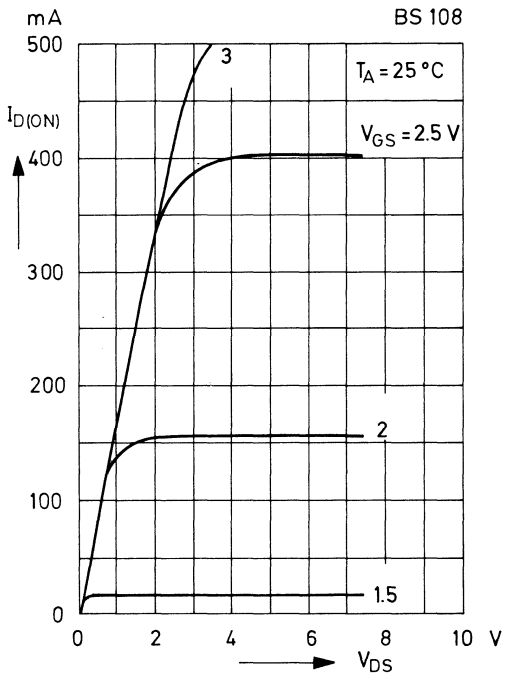
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%

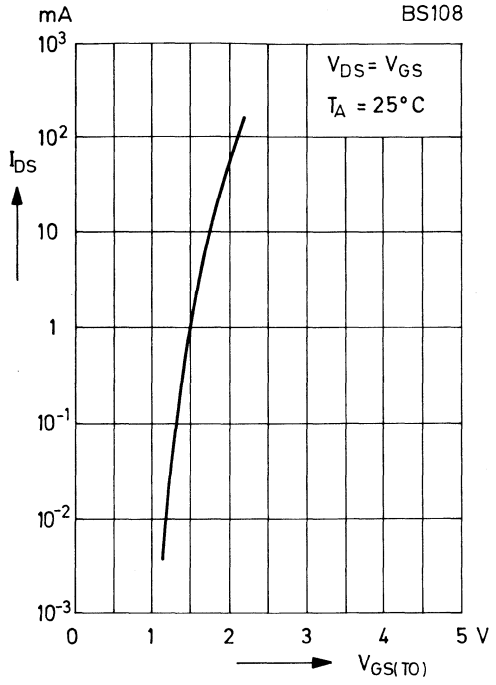


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%

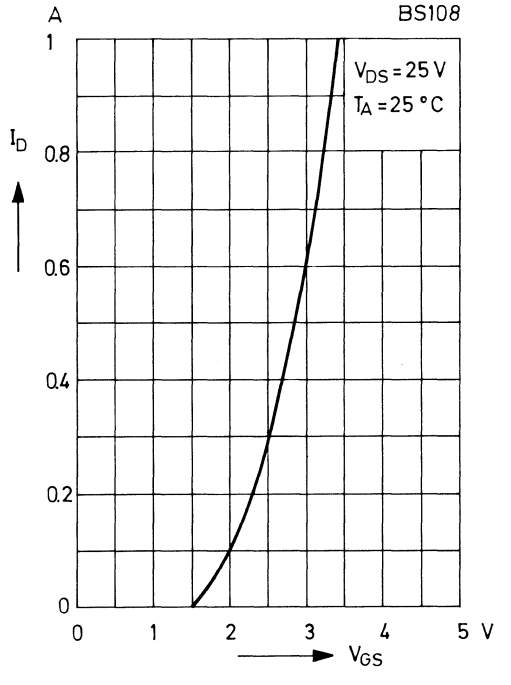


Drain-source current versus gate threshold voltage

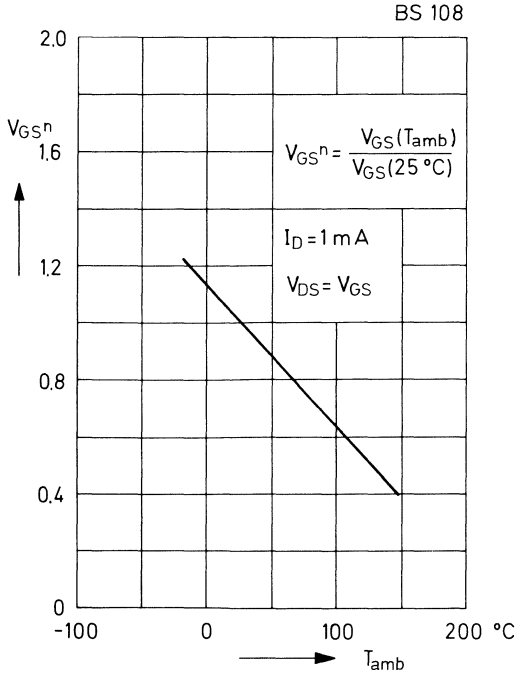


Drain current versus gate-source voltage

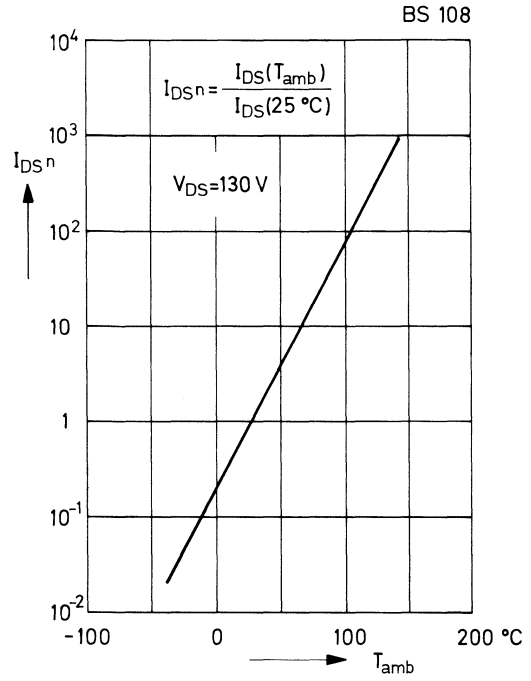
Pulse test width 80 μs; pulse duty factor 1%



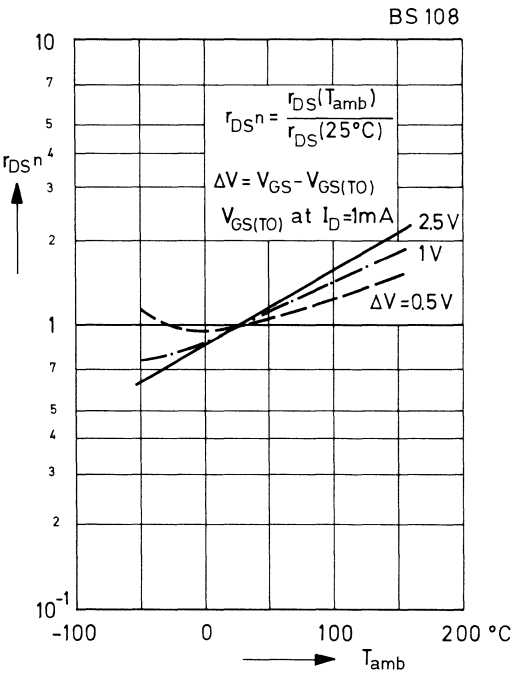
Normalized gate-source voltage versus temperature



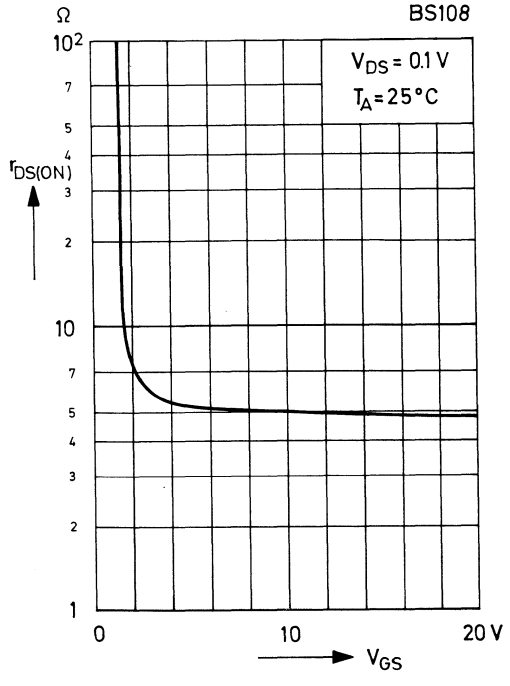
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

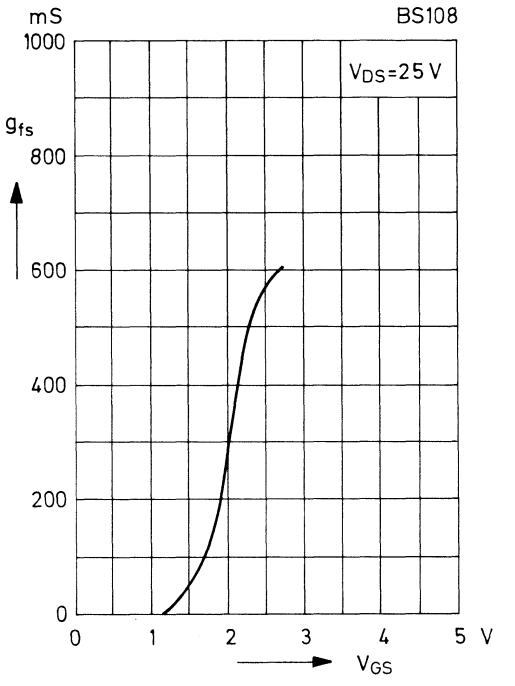


Drain-source resistance versus gate-source voltage



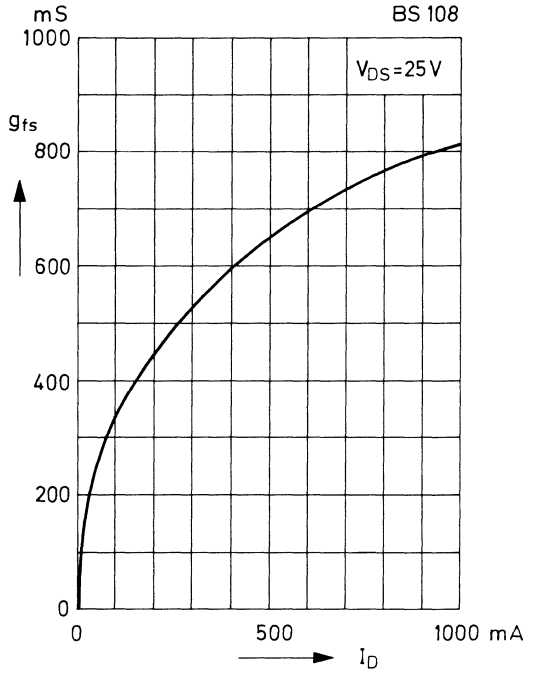
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%

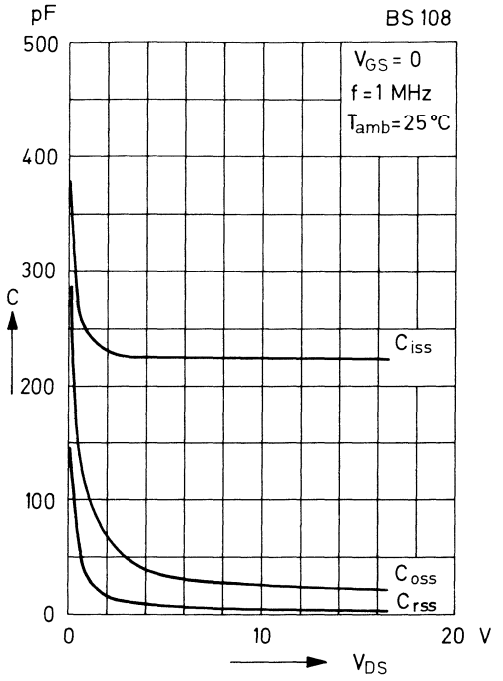


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%



Capacitance versus drain-source voltage



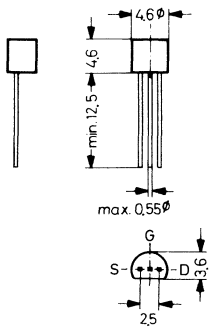
BS112

N-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	170	V
Drain Gate Voltage	V_{DGS}	170	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	200	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.75	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

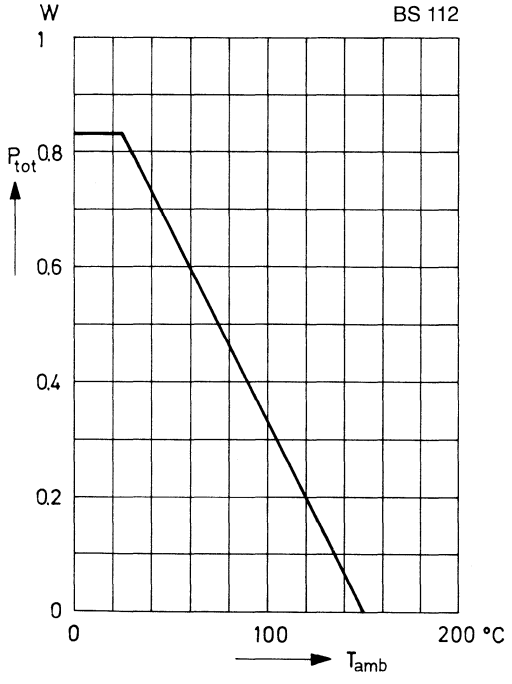
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu A$, $V_{GS} = 0$	$V_{(BR)DSS}$	170	190	–	V
Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$	I_{GSS}	–	–	10	nA
Drain Cutoff Current at $V_{DS} = 100$ V, $V_{GS} = 0$ at $V_{DS} = 70$ V, $V_{GS} = 0.2$ V	 I_{DSS} I_{DSX}	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS\,(TO)}$	–	1.5	2.5	V
Drain-Source ON Resistance at $V_{GS} = 2.8$ V, $I_D = 100$ mA	$r_{DS\,(ON)}$	–	5.5	10	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Capacitances at $V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 220 20 5	 – – –	 pF pF pF
Switching Times at $V_{GS} = 10$ V, $V_{DS} = 10$ V, $R_D = 100\ \Omega$ Turn On Time Turn Off Time	 t_{on} t_{off}	 – –	 5 50	 – –	 ns ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

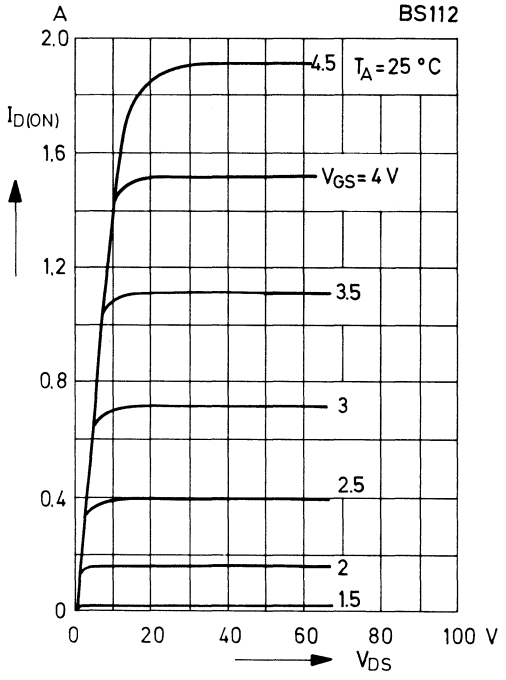
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



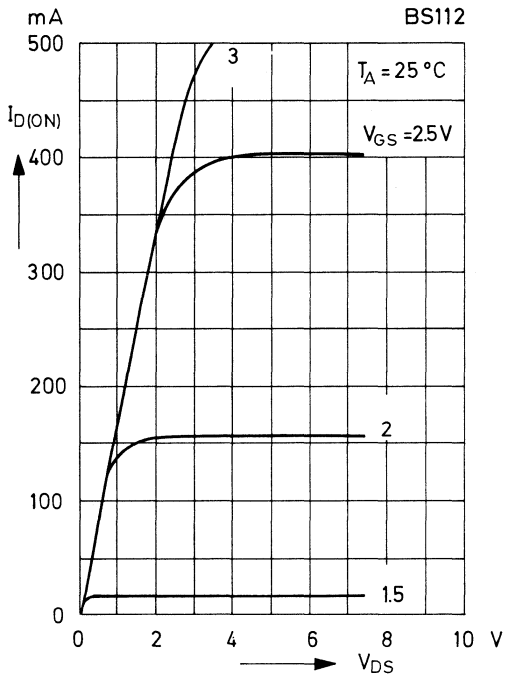
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%

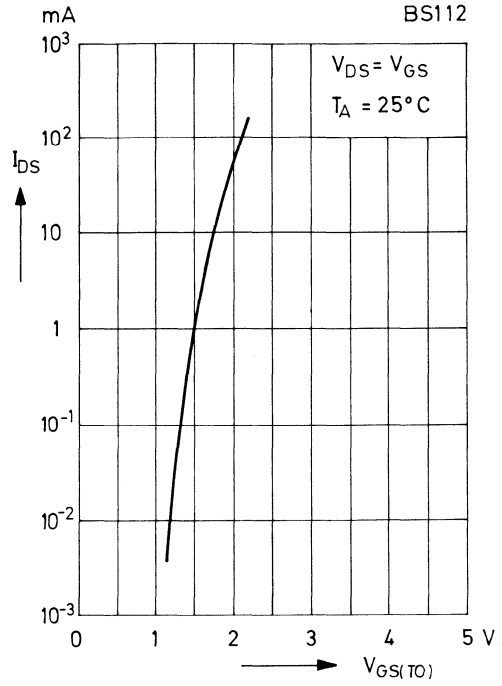


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%

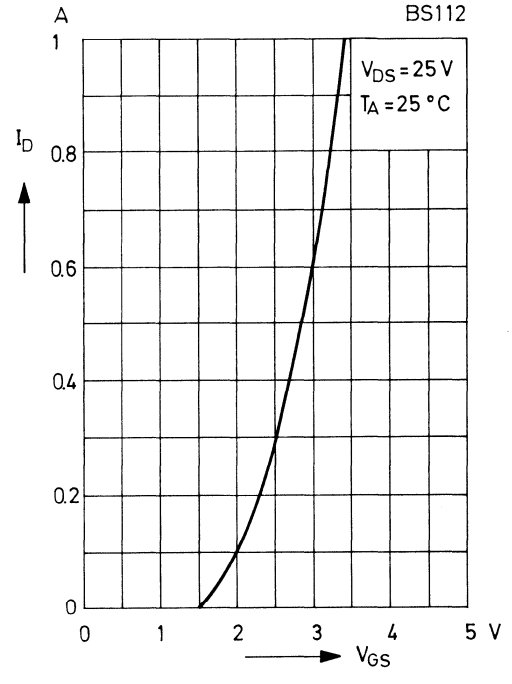


Drain-source current versus gate threshold voltage

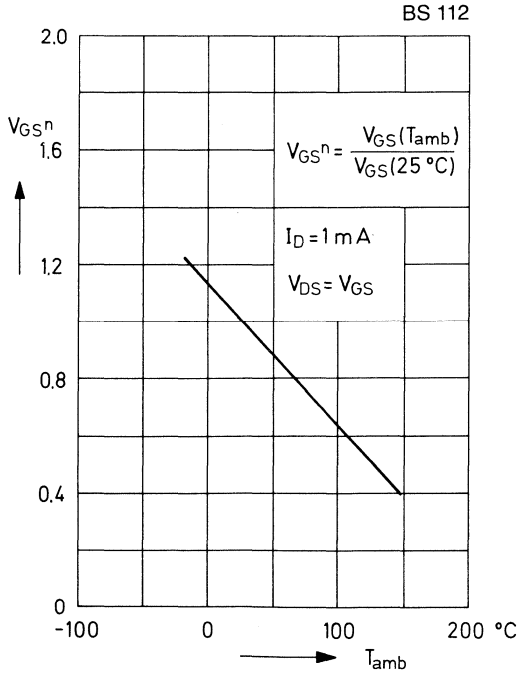


Drain current versus gate-source voltage

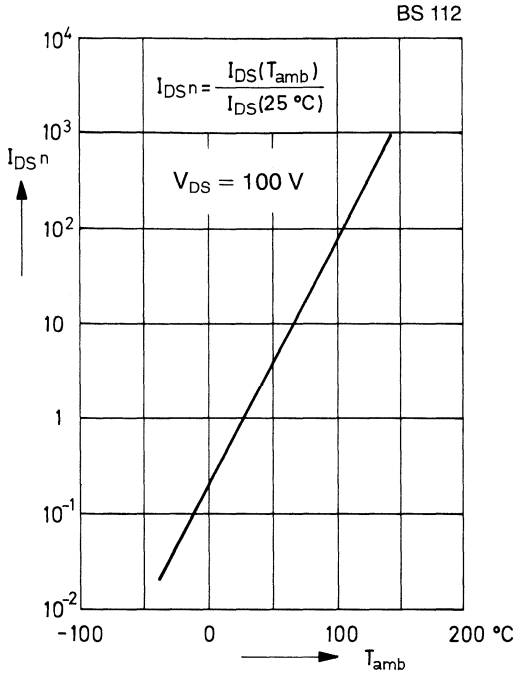
Pulse test width 80 μs; pulse duty factor 1%



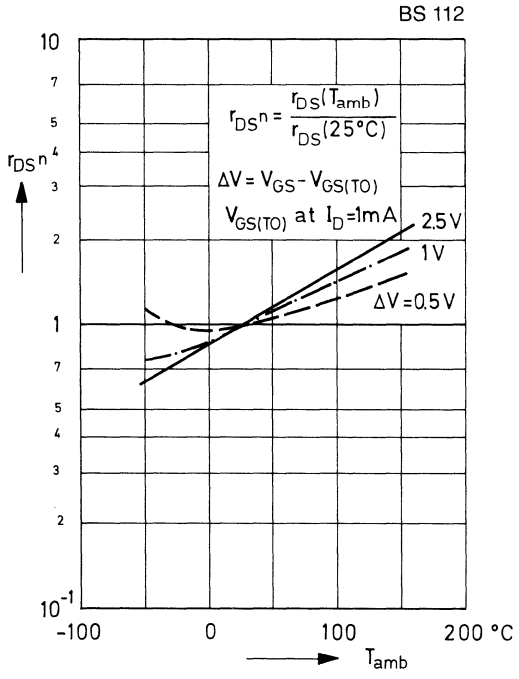
Normalized gate-source voltage versus temperature



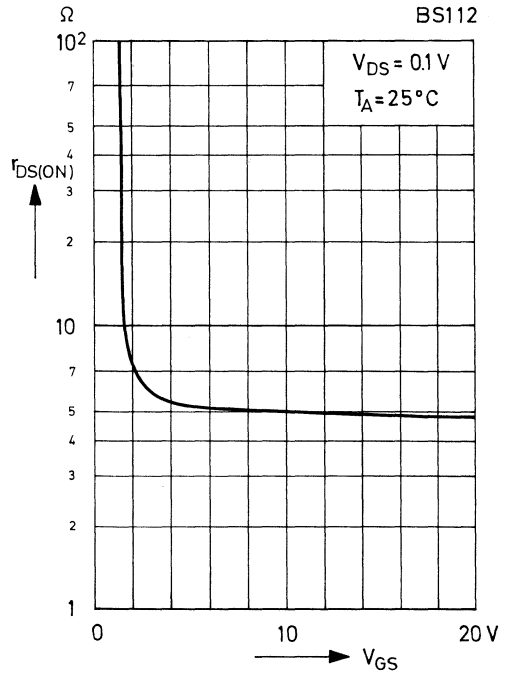
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

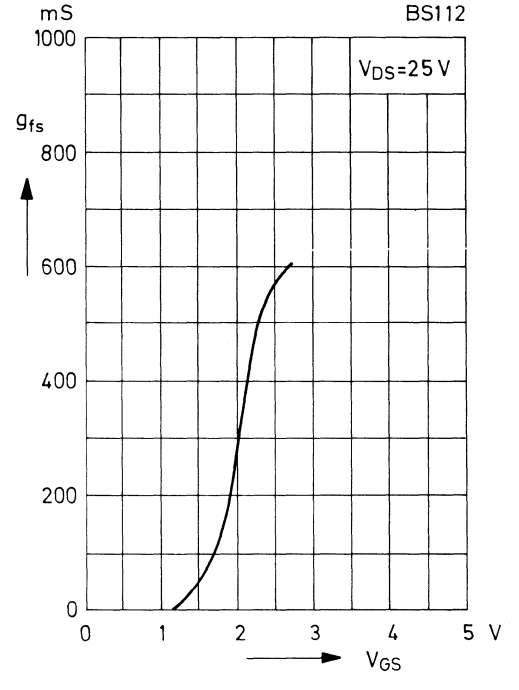


Drain-source resistance versus gate-source voltage



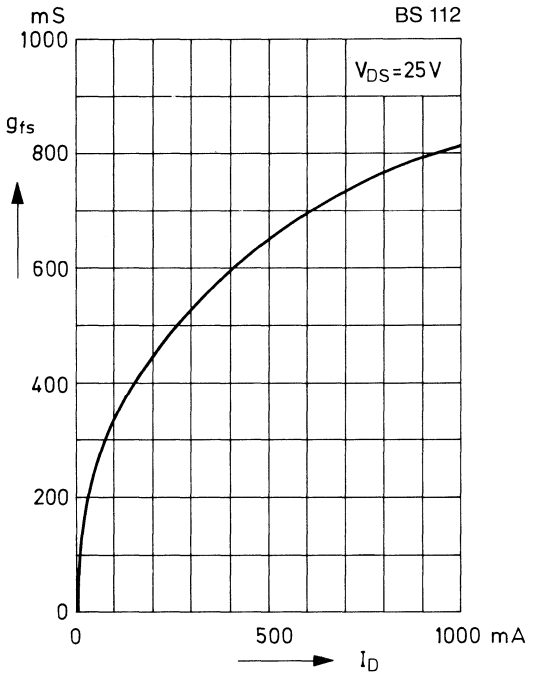
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%

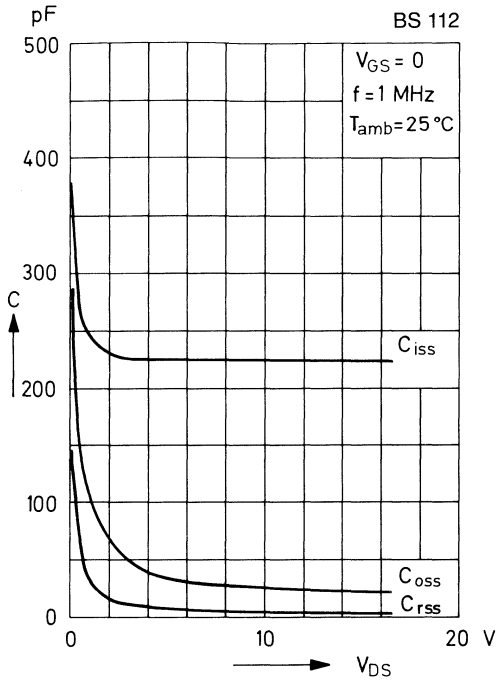


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%



Capacitance versus drain-source voltage

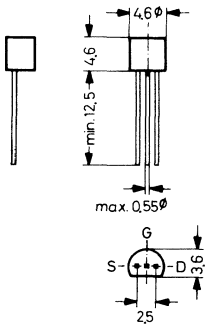


BS170

N-Channel Enhancement Mode VMOS Transistor

Features:
High input impedance
High speed switching
No minority carrier storage time
CMOS logic compatible input
No thermal runaway
No secondary breakdown

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGS}	60	V
Gate-Source-Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	300	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.5	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.5 A, T_j = 25 °C	V_F	0.85	V

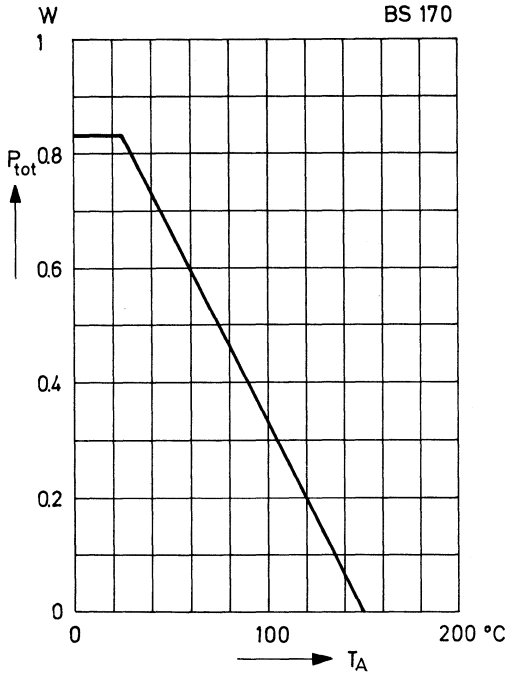
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu A$, $V_{GS} = 0$	$V_{(BR)DSS}$	60	90	–	V
Gate Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS(TO)}$	0.8	2	3.0	V
Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$	I_{GSS}	–	–	10	nA
Drain-Cutoff Current at $V_{DS} = 25$ V, $V_{GS} = 0$	I_{DSS}	–	–	0.5	μA
Drain-Source ON Resistance at $V_{GS} = 10$ V, $I_D = 0.2$ mA	$r_{DS\ (ON)}$	–	3.5	5.0	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Forward Transconductance at $V_{DS} = 10$ V, $I_D = 0.2$ A, f = 1 MHz	g_m	–	200	–	mS
Input Capacitance at $V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 MHz	C_{iss}	–	60	–	pF
Switching Times at $V_{GS} = 10$ V, $V_{DS} = 10$ V, $R_D = 100\ \Omega$					
Turn On Time	t_{on}	–	5	–	ns
Turn Off Time	t_{off}	–	15	–	ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

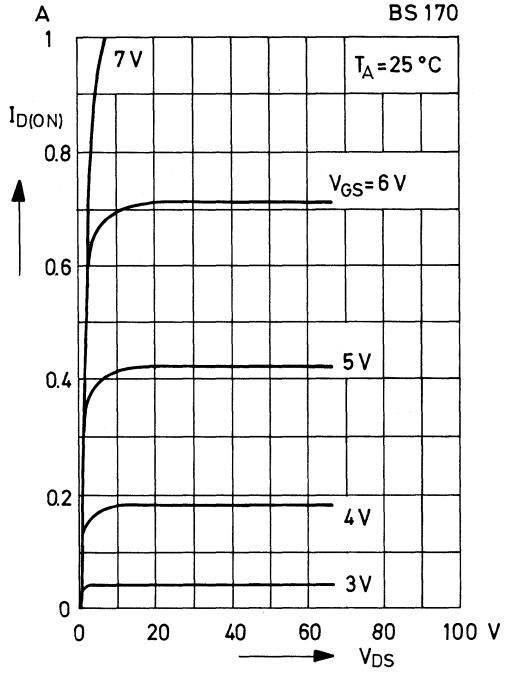
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



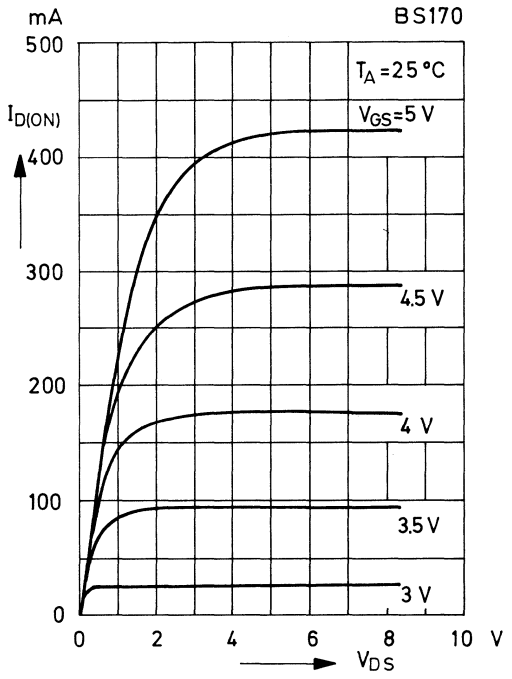
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%.

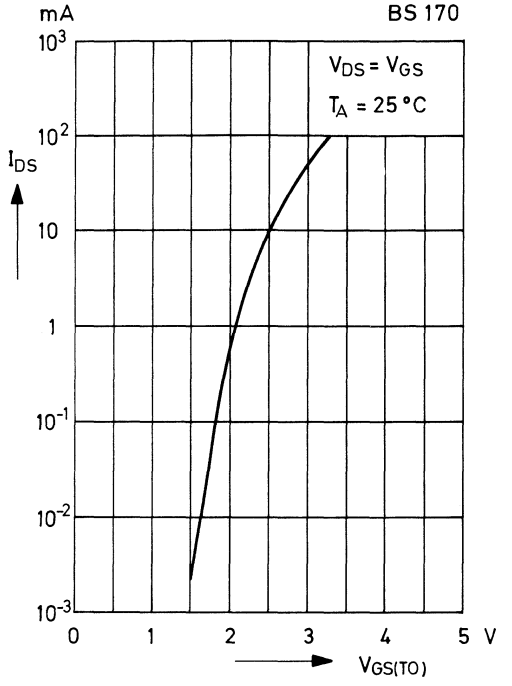


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%.

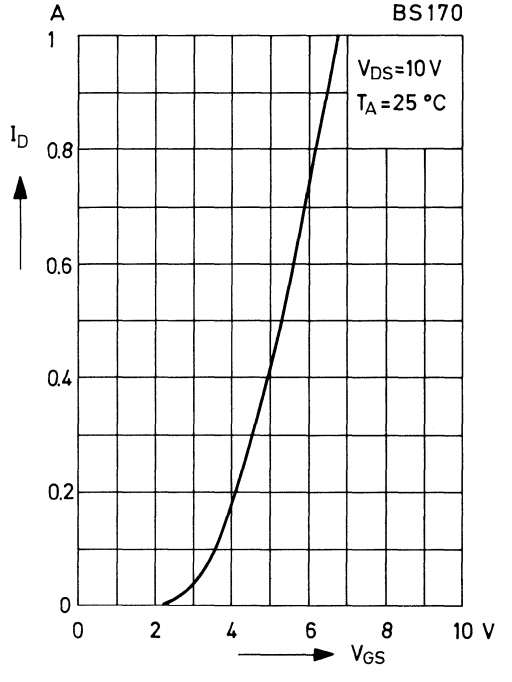


Drain-source current versus gate threshold voltage

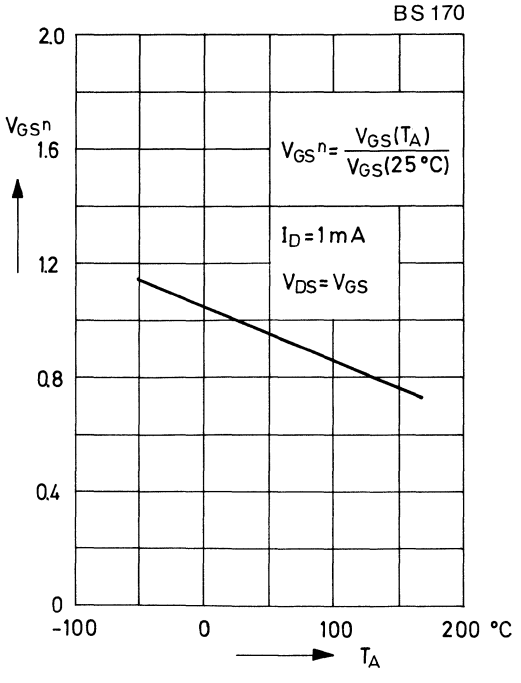


Drain current versus gate-source voltage

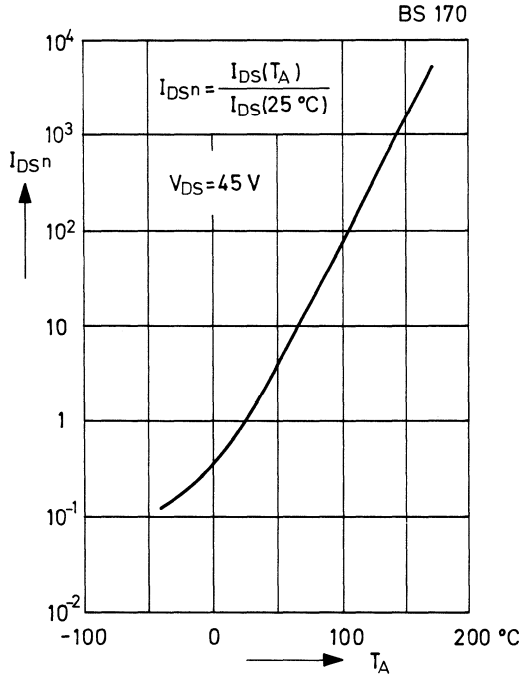
Pulse test width 80 μs; pulse duty factor 1%.



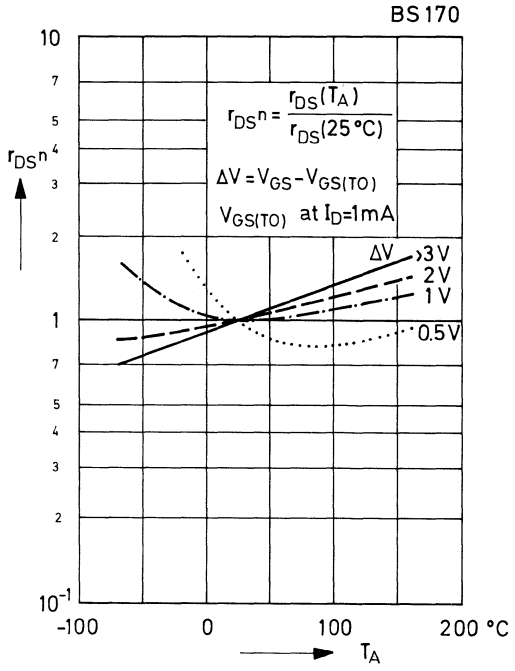
Normalized gate-source voltage versus temperature



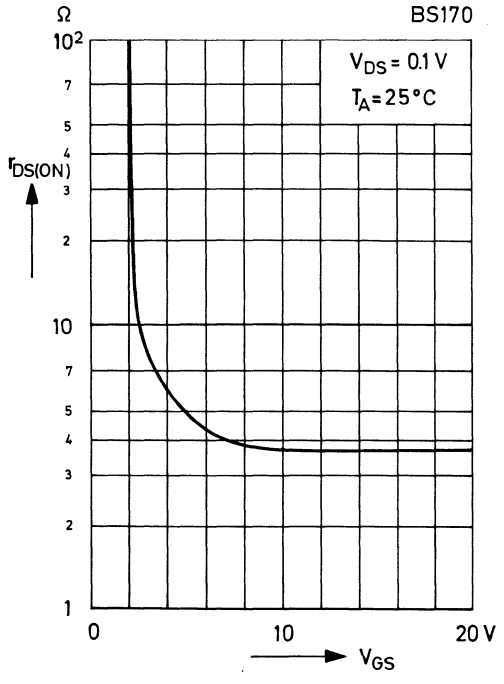
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

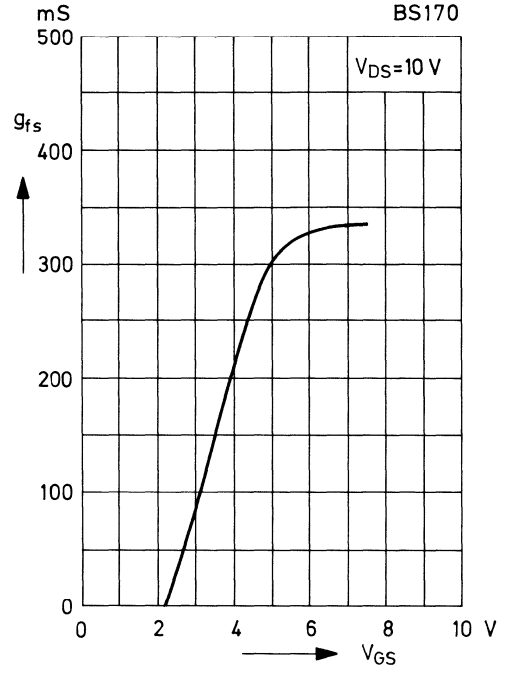


Drain-source resistance versus gate-source voltage



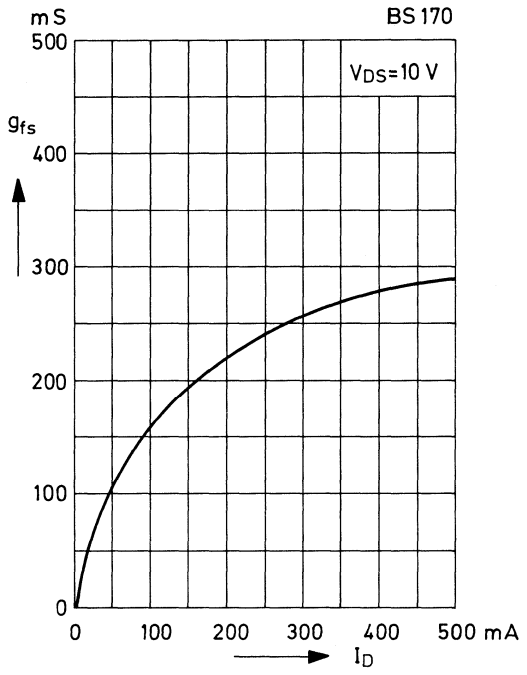
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%.

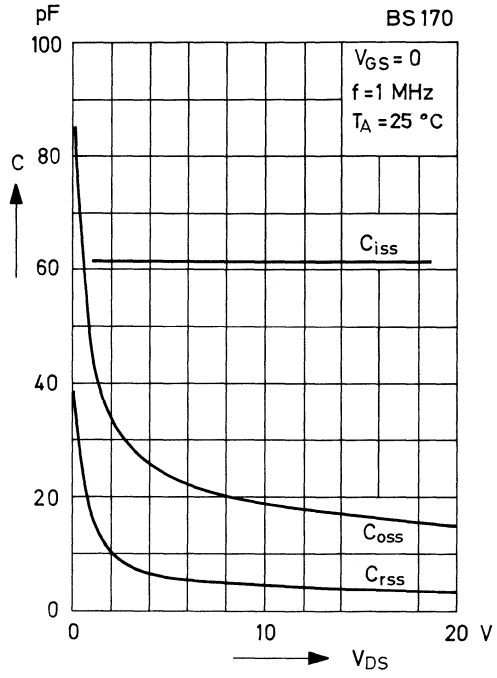


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%



Capacitance versus drain-source voltage



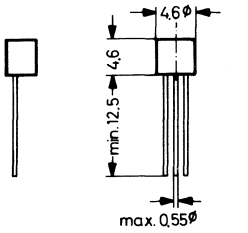
BS189

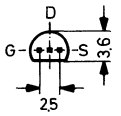
N-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.





Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	200	V
Drain Gate Voltage	V_{DGS}	200	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	I_D	250	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.22	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

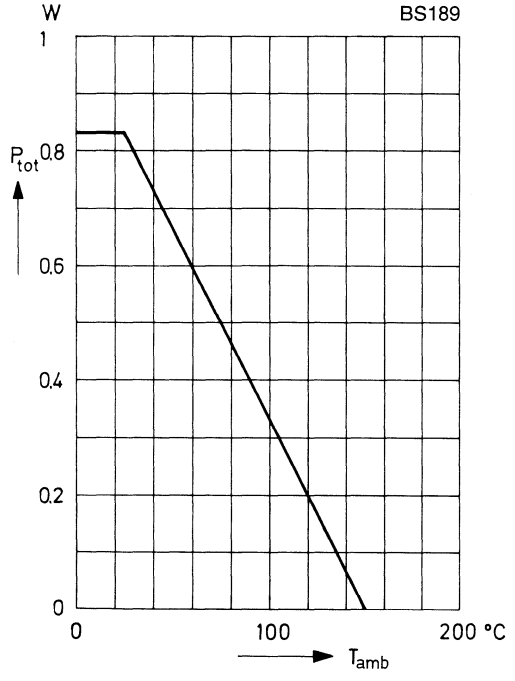
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 100\ \mu A$, $V_{GS} = 0$	$V_{(BR)DSS}$	200	230	–	V
Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$	I_{GSS}	–	–	10	nA
Drain Cutoff Current at $V_{DS} = 130$ V, $V_{GS} = 0$ at $V_{DS} = 10$ V, $V_{GS} = 0.2$ V	 I_{DSS} I_{DSX}	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA	$V_{GS\,(TO)}$	–	1.5	2.5	V
Drain-Source ON Resistance at $V_{GS} = 5$ V, $I_D = 100$ mA	$r_{DS\,(ON)}$	–	4.5	7	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Capacitances at $V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 220 20 2	 – – –	 pF pF pF
Switching Times at $V_{GS} = 10$ V, $V_{DS} = 10$ V, $R_D = 100\ \Omega$ Turn On Time Turn Off Time	 t_{on} t_{off}	 – –	 5 50	 – –	 ns ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

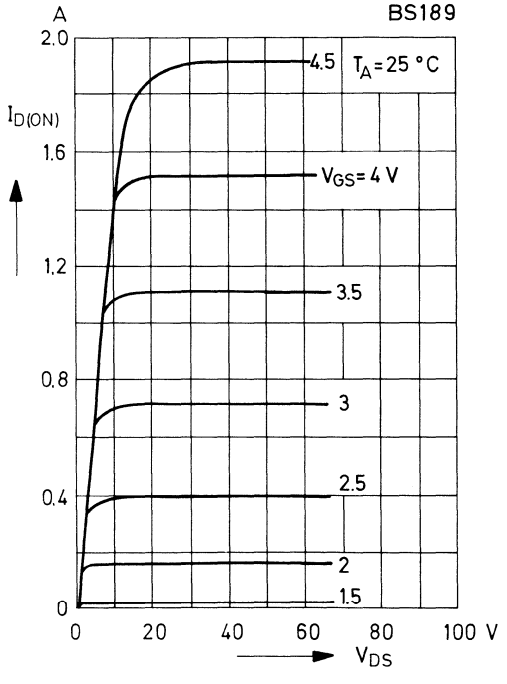
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



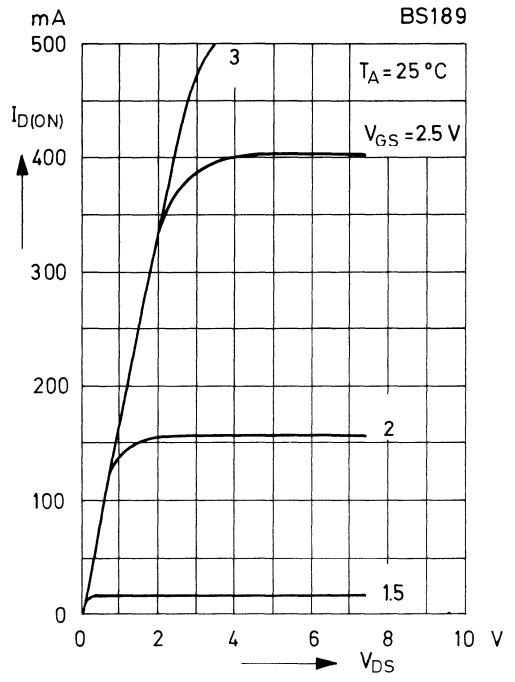
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%

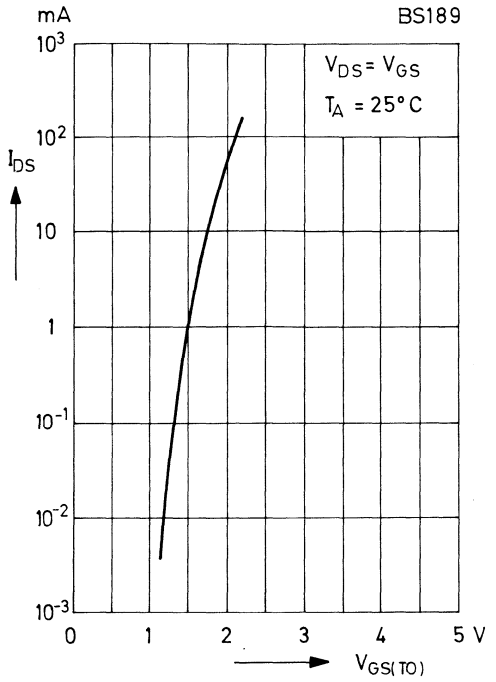


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%

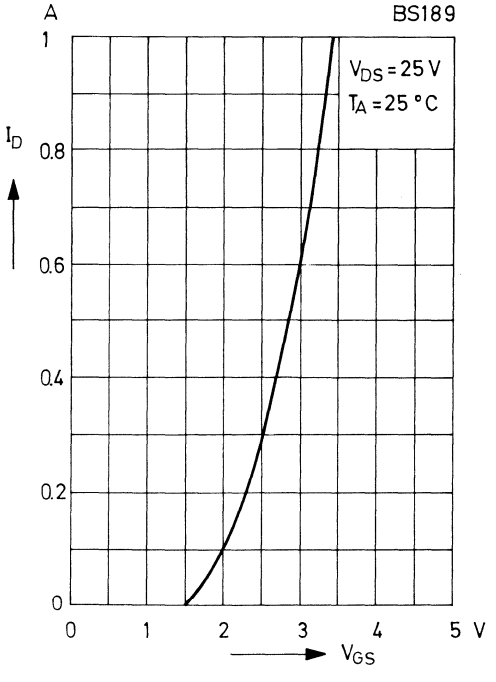


Drain-source current versus gate threshold voltage

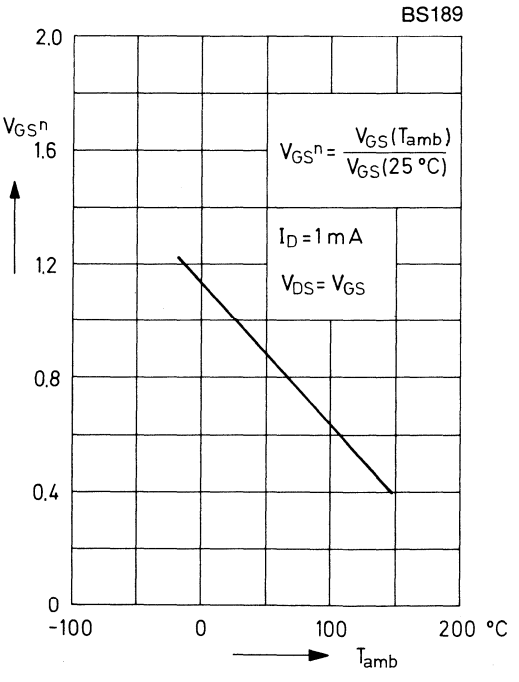


Drain current versus gate-source voltage

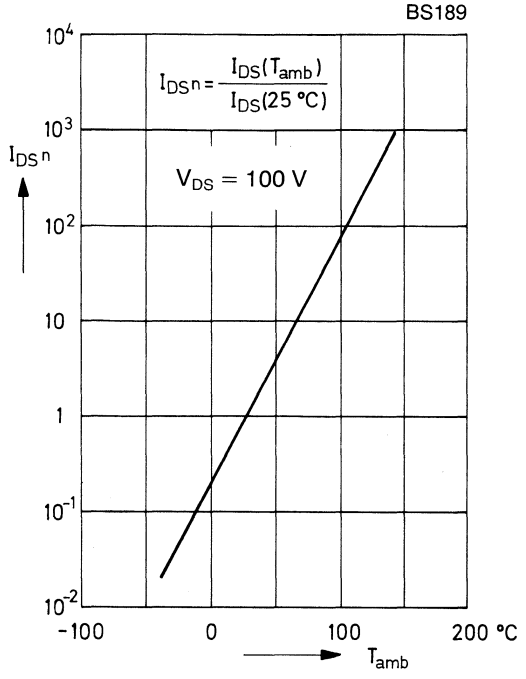
Pulse test width 80 μs; pulse duty factor 1%



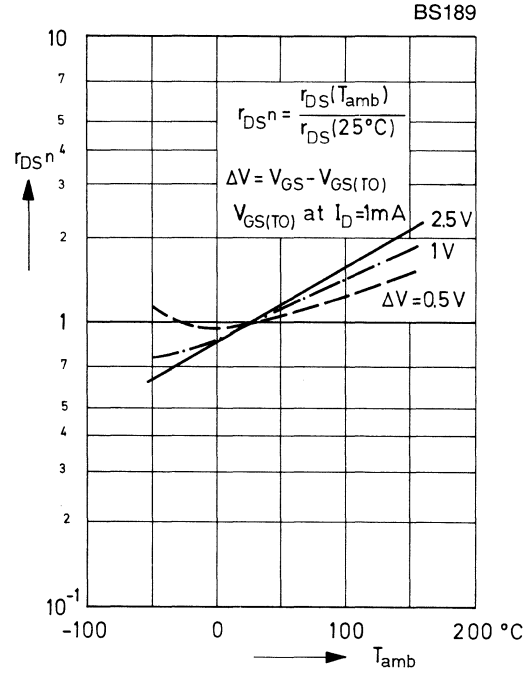
Normalized gate-source voltage versus temperature



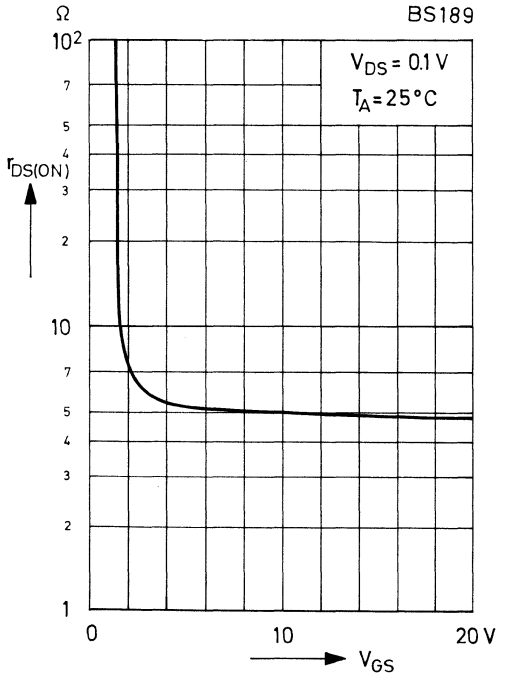
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

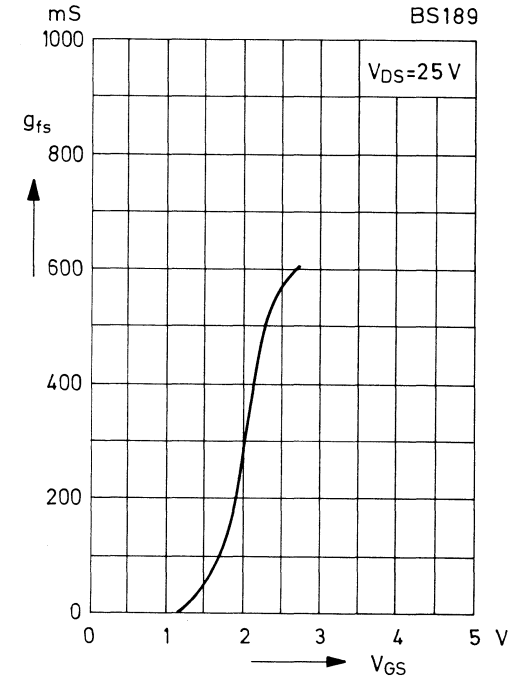


Drain-source resistance versus gate-source voltage



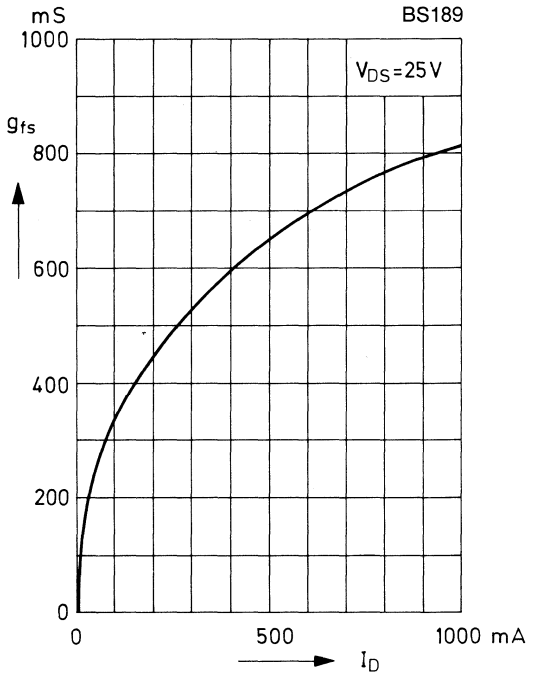
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1 %

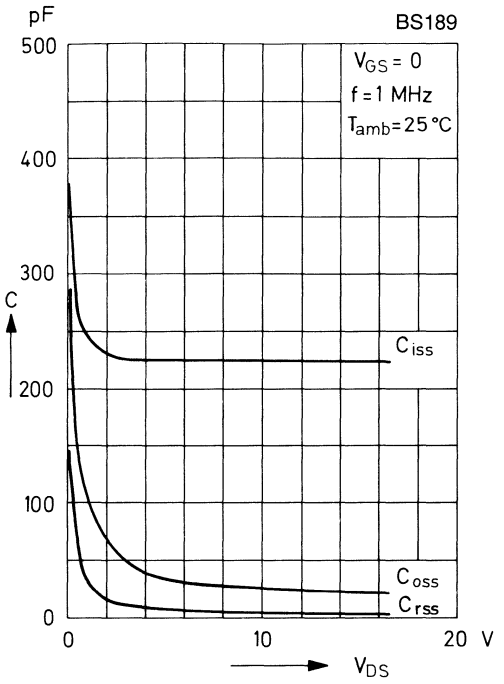


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%



Capacitance versus drain-source voltage



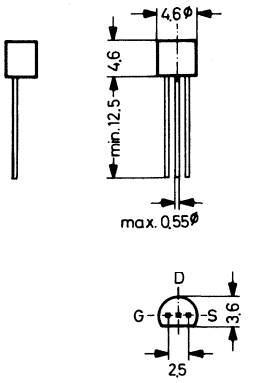
BS192

P-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	200	V
Drain-Gate Voltage	$-V_{DGS}$	200	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Curent (continuous)	$-I_D$	180	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 to +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.22	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

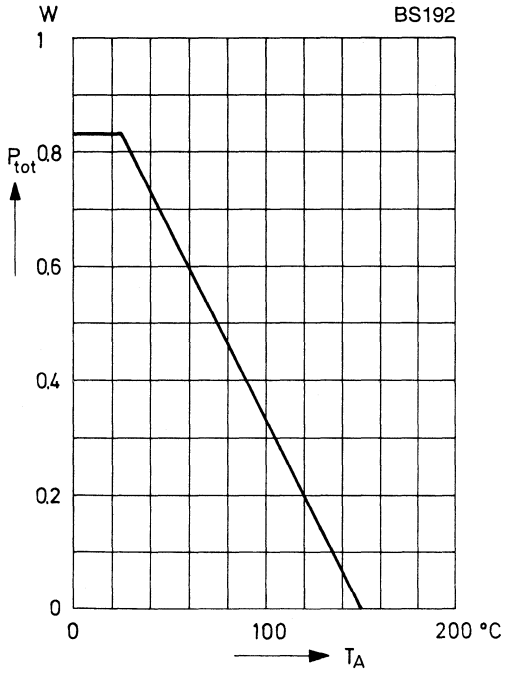
Characteristics at T_j = 25 °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D$ = 100 μA, V_{GS} = 0	$-V_{(BR)DSS}$	200	230	–	V
Gate-Body Leakage Current at $-V_{GS}$ = 15 V, V_{DS} = 0	$-I_{GSS}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS}$ = 130 V, V_{GS} = 0 at $-V_{DS}$ = 70 V, $-V_{GS}$ = 0.2 V	 $-I_{DSS}$ $-I_{DSX}$	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at V_{GS} = V_{DS}, $-I_D$ = 1 mA	$-V_{GS\,(TO)}$	–	2.8	4	V
Drain-Source ON Resistance at $-V_{GS}$ = 10 V, $-I_D$ = 100 mA	$r_{DS\,(ON)}$	–	7	14	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1]	K/W
Capacitances at $-V_{DS}$ = 20 V, V_{GS} = 0, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 270 35 6	 – – –	 pF pF pF
Switching Times at $-I_D$ = 200 mA, $-U_{GS}$ = 10 V Turn On Time Storage Time Fall Time	 t_{on} t_s t_f	 – – –	 5 20 15	 – – –	 ns ns ns

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

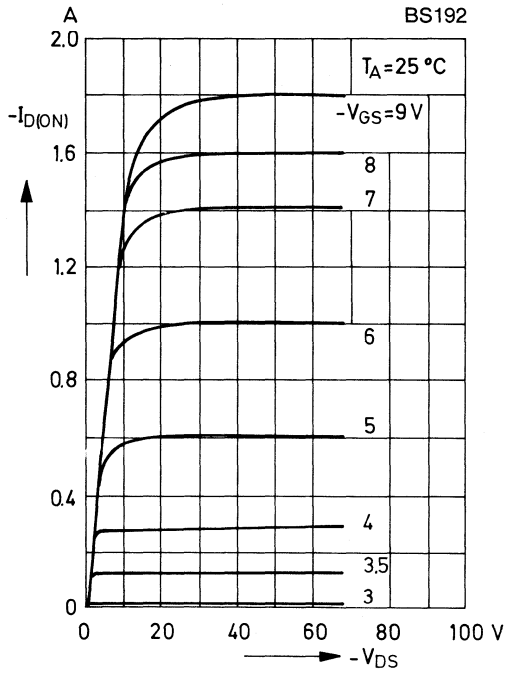
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



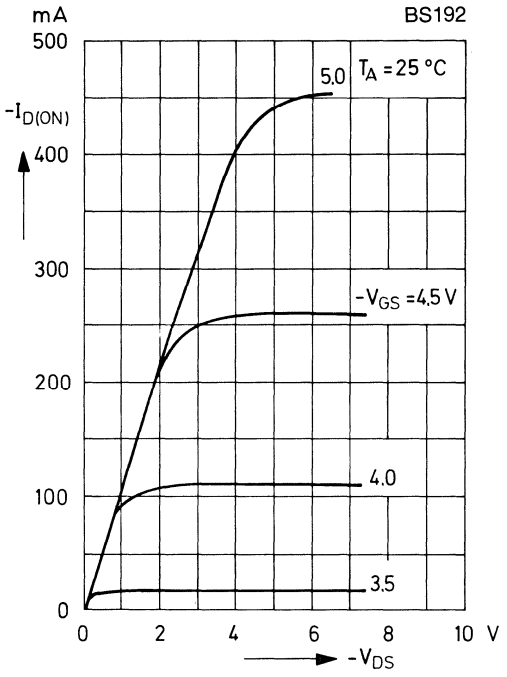
Output characteristics

Pulse test width 80 μs; pulse duty factor 1 %

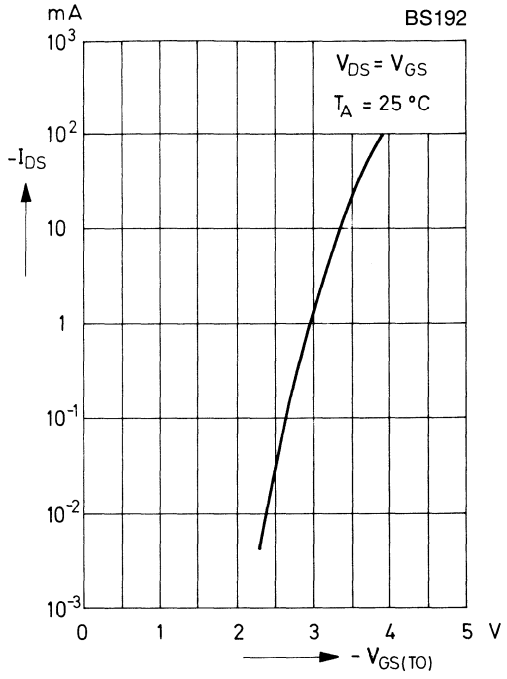


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%.

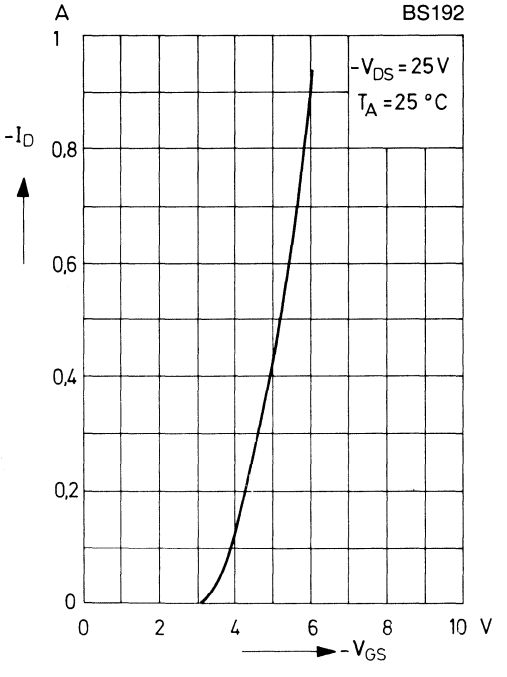


Drain-source current versus gate threshold voltage

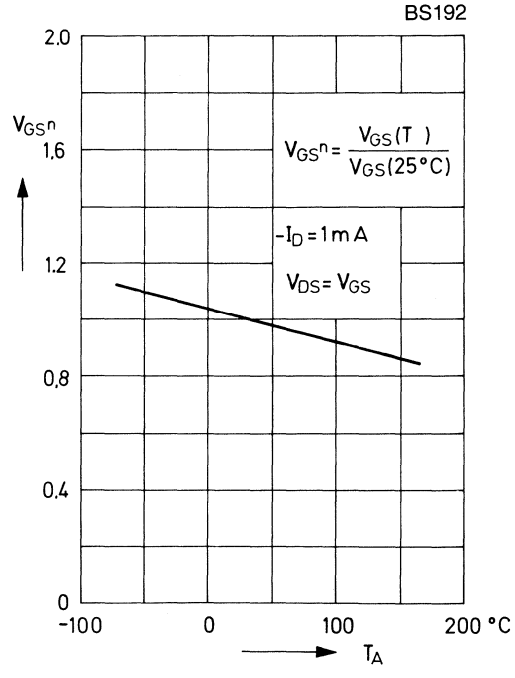


Drain current versus gate-source voltage

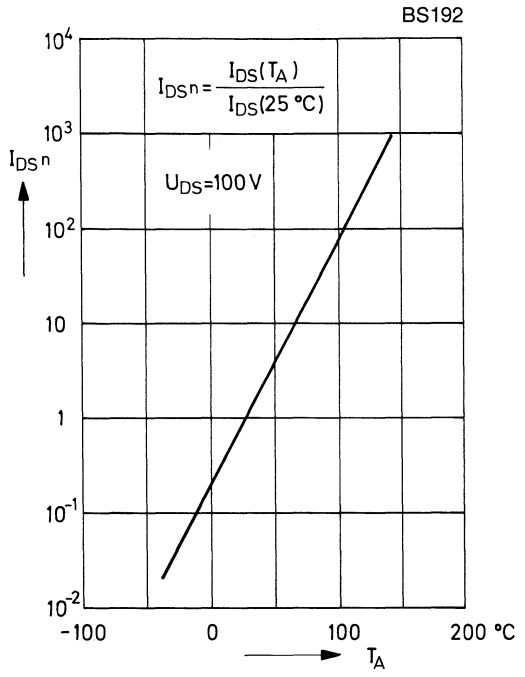
Pulse test width 80 μs; pulse duty factor 1%.



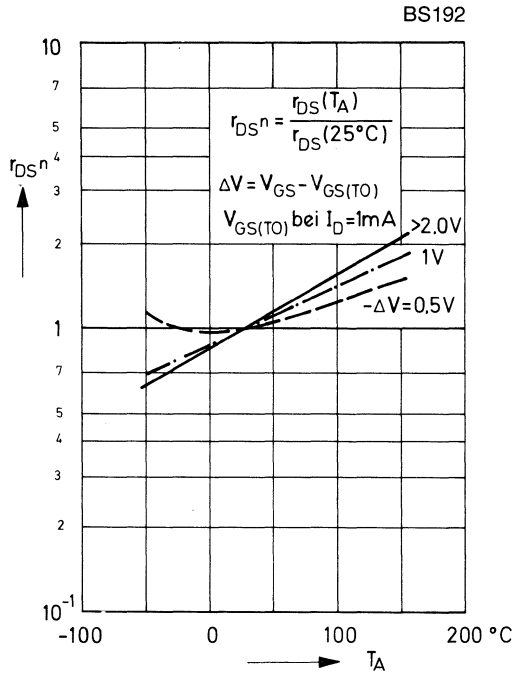
Normalized gate-source voltage versus temperature



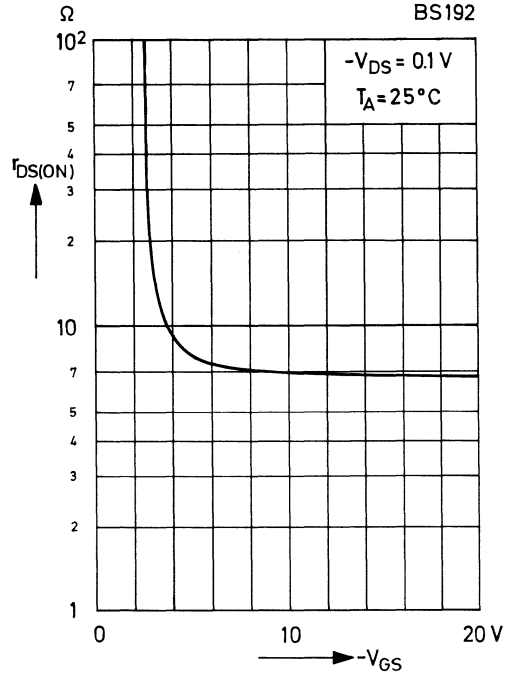
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

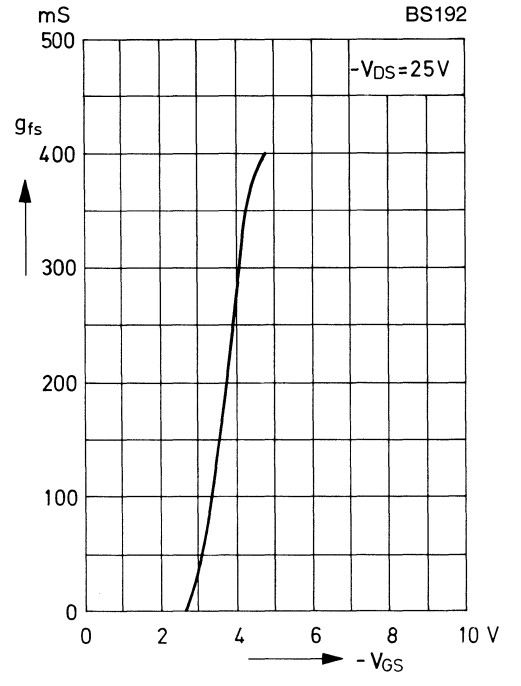


Drain-source resistance versus gate-source voltage



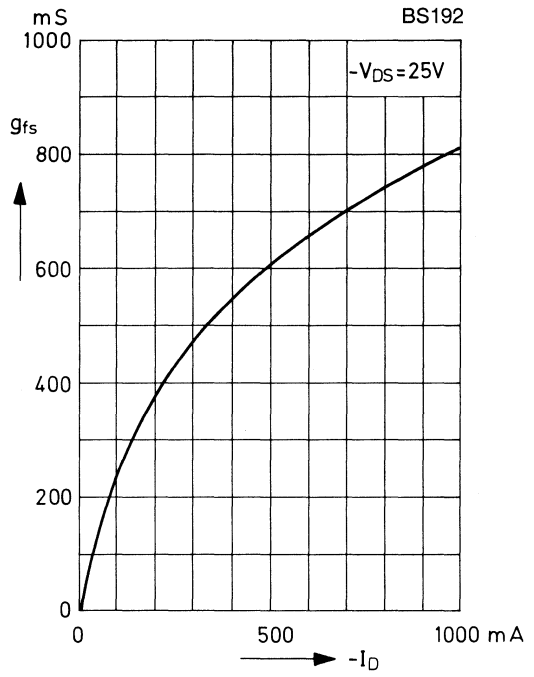
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%.

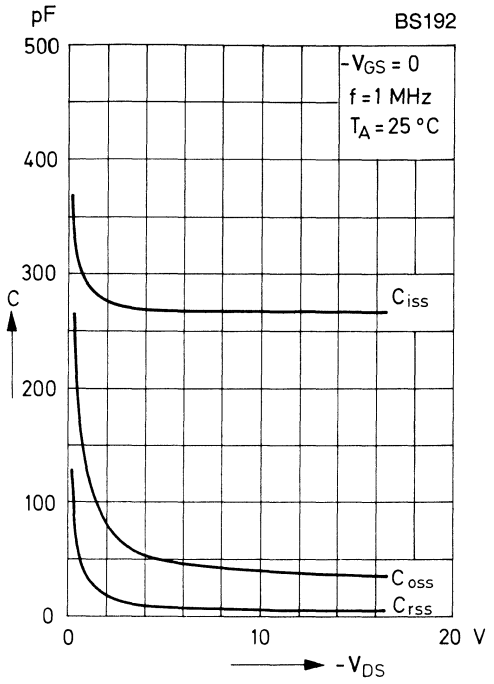


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%.



Capacitance versus drain-source voltage



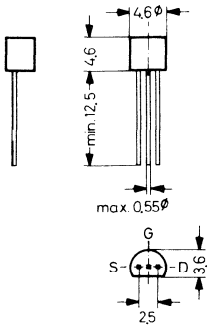
BS208

P-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain Source Voltage	$-V_{DSS}$	200	V
Drain-Gate Voltage	$-V_{DGS}$	200	V
Gate-Source Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	$-I_D$	200	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.22	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

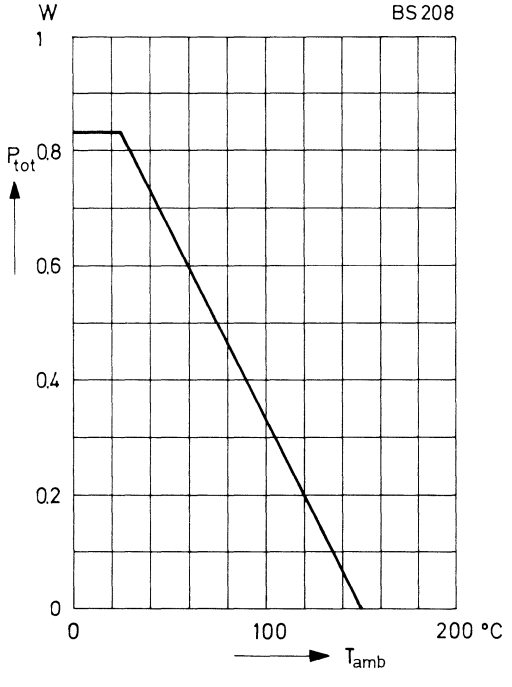
Characteristics at $T_j = 25\ °C$

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D = 100\ \mu A$, $V_{GS} = 0$	$-V_{(BR)DSS}$	200	230	–	V
Gate-Body Leakage Current at $-V_{GS} = 15$ V, $V_{DS} = 0$	$-I_{GSS}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS} = 130$ V, $V_{GS} = 0$ at $-V_{DS} = 10$ V, $-V_{GS} = 0.2$ V	 $-I_{DSS}$ $-I_{DSX}$	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D = 1$ mA	$-V_{GS\,(TO)}$	–	2.8	4	V
Drain-Source ON Resistance at $-V_{GS} = 5$ V, $-I_D = 100$ mA	$r_{DS\,(ON)}$	–	7	14	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1]	K/W
Capacitances at $-V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 270 35 6	 – – –	 pF pF pF
Switching Times at $-I_D = 200$ mA, $-U_{GS} = 10$ V Turn On Time Storage Time Fall Time	 t_{on} t_s t_f	 – – –	 5 20 15	 – – –	 ns ns ns

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

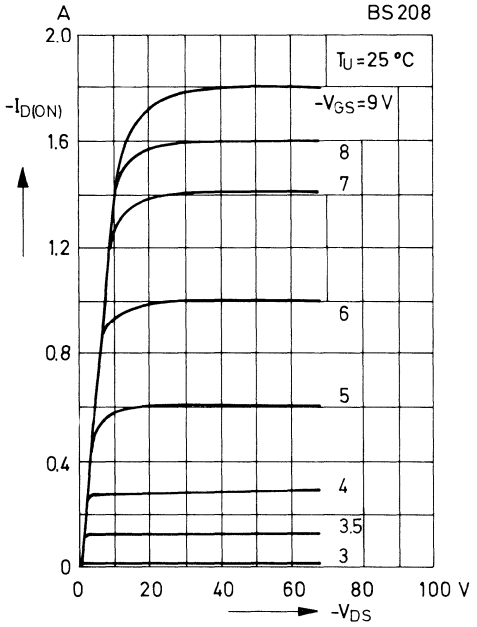
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



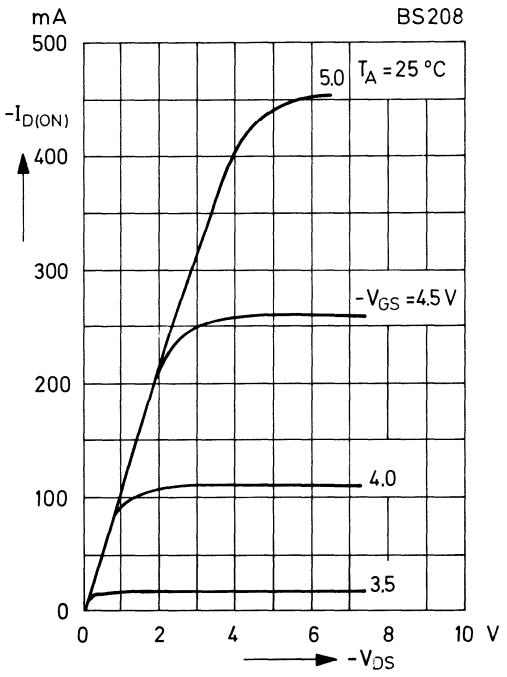
Output characteristics

Pulse test width 80 μs; pulse duty factor 1 %

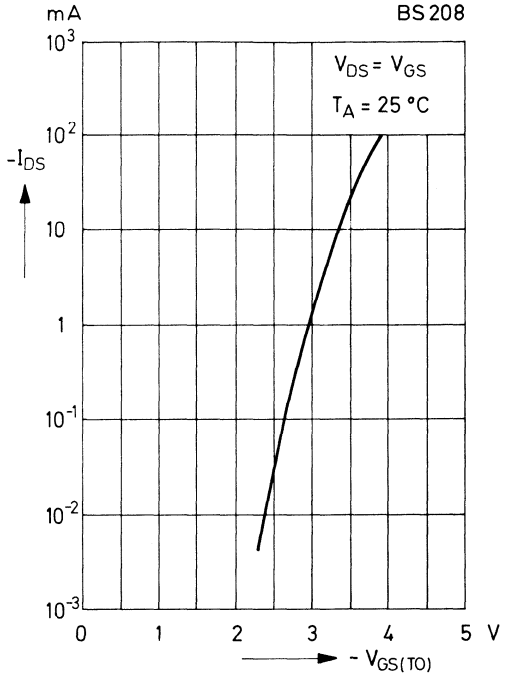


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%.

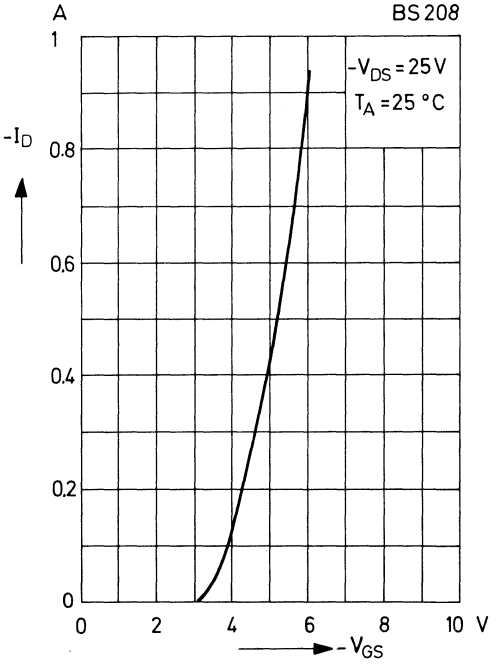


Drain-source current versus gate threshold voltage

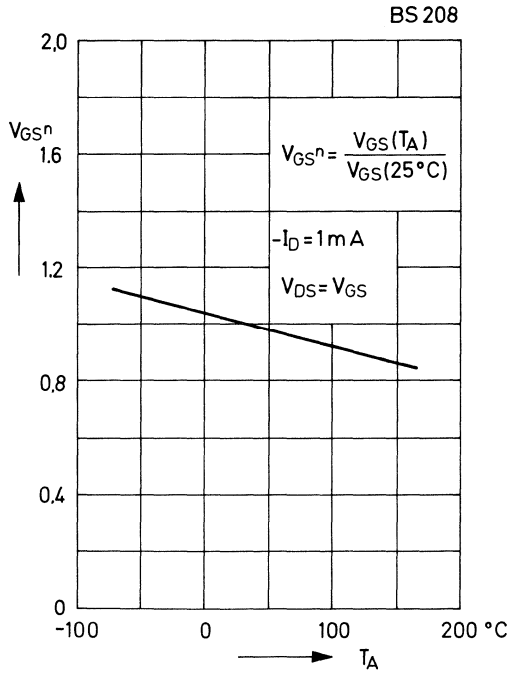


Drain current versus gate-source voltage

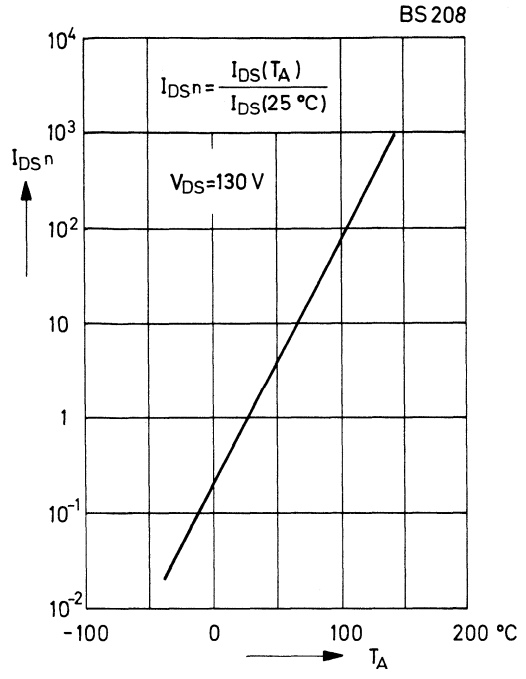
Pulse test width 80 μs; pulse duty factor 1%.



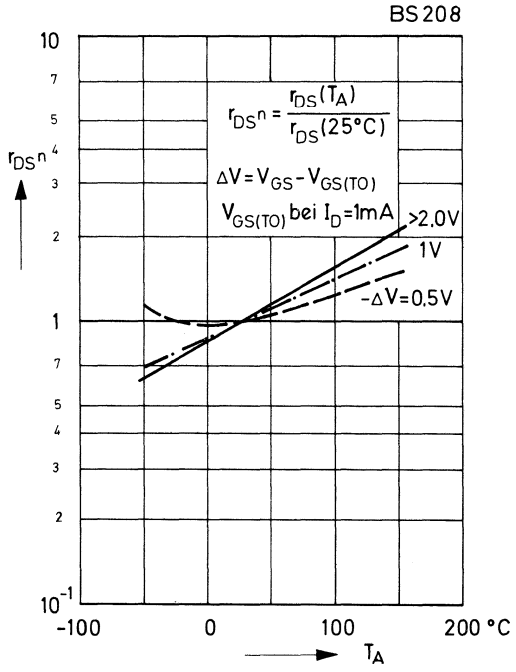
Normalized gate-source voltage versus temperature



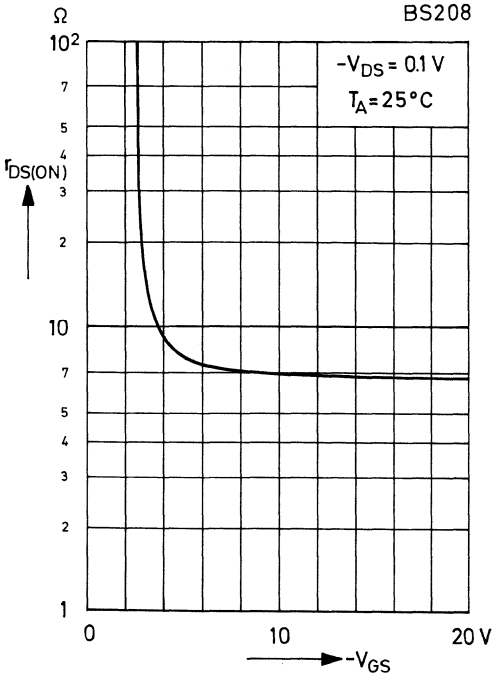
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

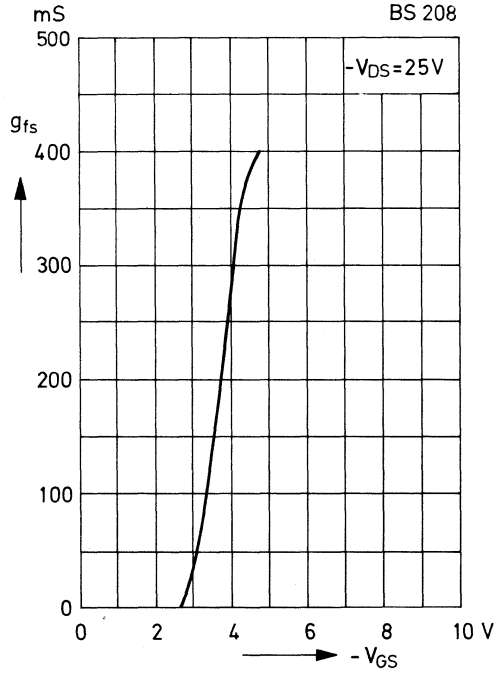


Drain-source resistance versus gate-source voltage



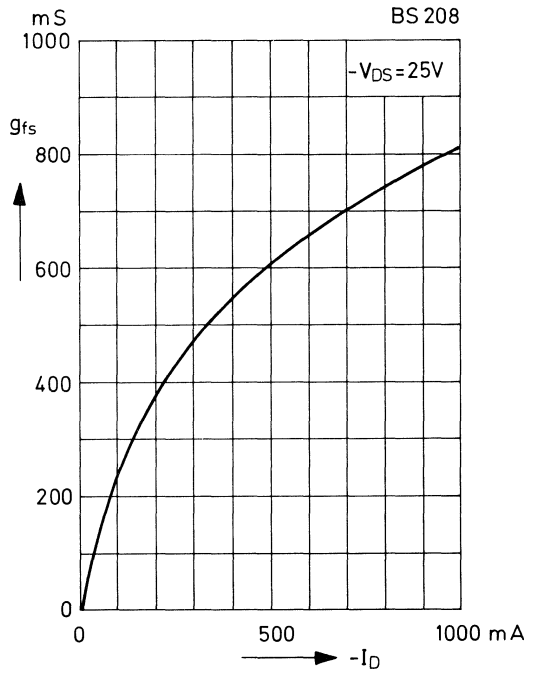
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%.

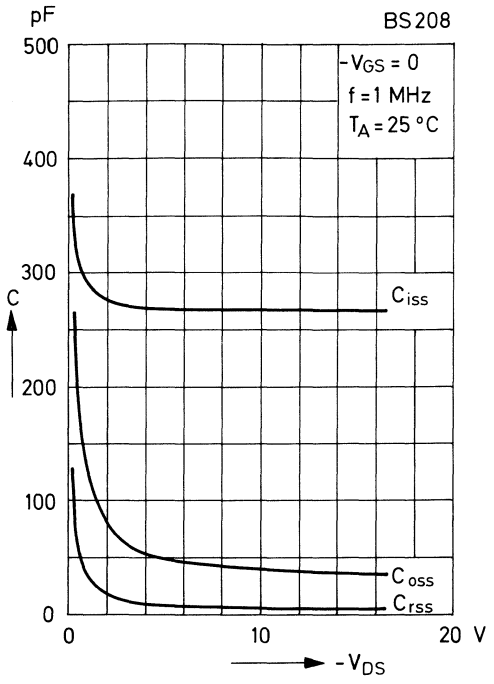


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%.



Capacitance versus drain-source voltage



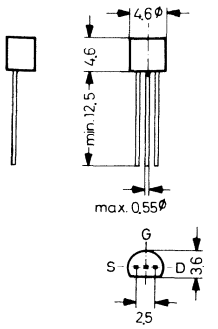
BS212

P-Channel Enhancement Mode VMOS Transistor

Features:

- high breakdown voltage
- high input impedance
- low gate threshold voltage
- low drain-source ON resistance
- high speed switching
- no minority carrier storage time
- CMOS logic compatible input
- no thermal runaway
- no secondary breakdown
- specially suited for telephone subsets

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source-Voltage	$-V_{DSS}$	170	V
Drain-Gate-Voltage	$-V_{DGS}$	170	V
Gate-Source-Voltage (pulsed)	V_{GS}	±20	V
Drain-Current (continuous)	$-I_D$	200	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.22	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.75 A, T_j = 25 °C	V_F	0.85	V

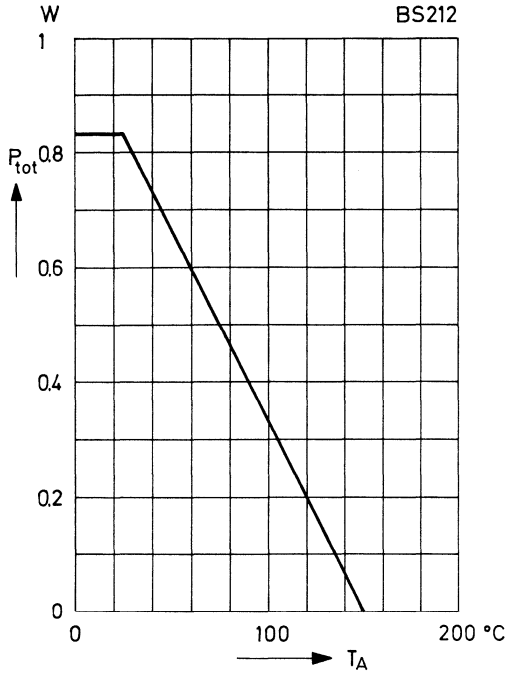
Characteristics at $T_j = 25$ °C

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D = 100\ \mu A$, $V_{GS} = 0$	$-V_{(BR)DSS}$	170	190	–	V
Gate-Body Leakage Current at $-V_{GS} = 15$ V, $V_{DS} = 0$	$-I_{GSS}$	–	–	10	nA
Drain Cutoff Current at $-V_{DS} = 100$ V, $V_{GS} = 0$ at $-V_{DS} = 70$ V, $-V_{GS} = 0.2$ V	 $-I_{DSS}$ $-I_{DSX}$	 – –	 – –	 1 25	 μA μA
Gate-Source Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D = 1$ mA	$-V_{GS\,(TO)}$	–	2.8	4	V
Drain-Source ON Resistance at $-V_{GS} = 10$ V, $-I_D = 100$ mA	$r_{DS\,(ON)}$	–	7	14	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1)]	K/W
Capacitances at $-V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz Input Capacitance Output Capacitance Feedback Capacitance	 C_{iss} C_{oss} C_{rss}	 – – –	 270 35 6	 – – –	 pF pF pF
Switching Times at $-I_D = 200$ mA, $-U_{GS} = 10$ V Turn On Time Storage Time Fall Time	 t_{on} t_s t_f	 – – –	 5 20 15	 – – –	 ns ns ns

[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

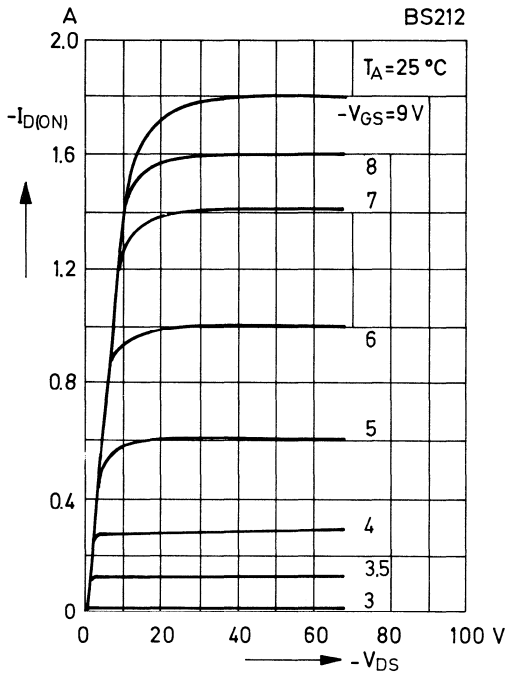
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



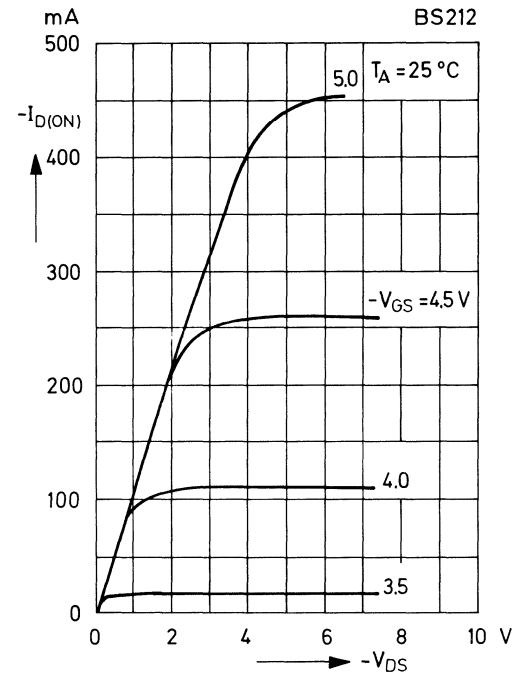
Output characteristics

Pulse test width 80 μs; pulse duty factor 1 %

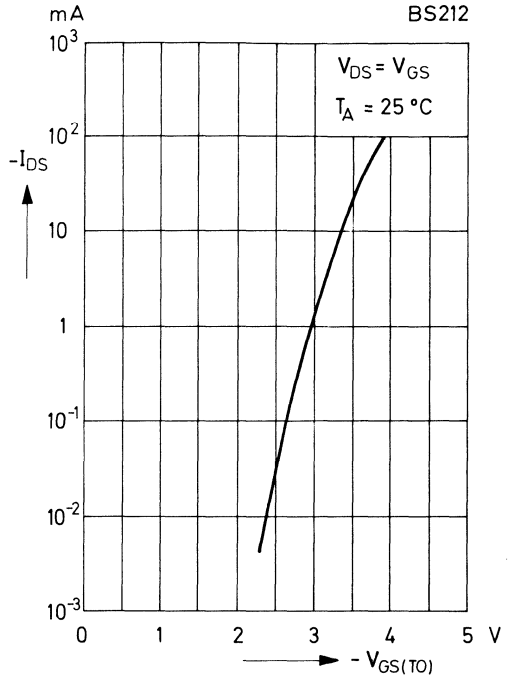


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%.

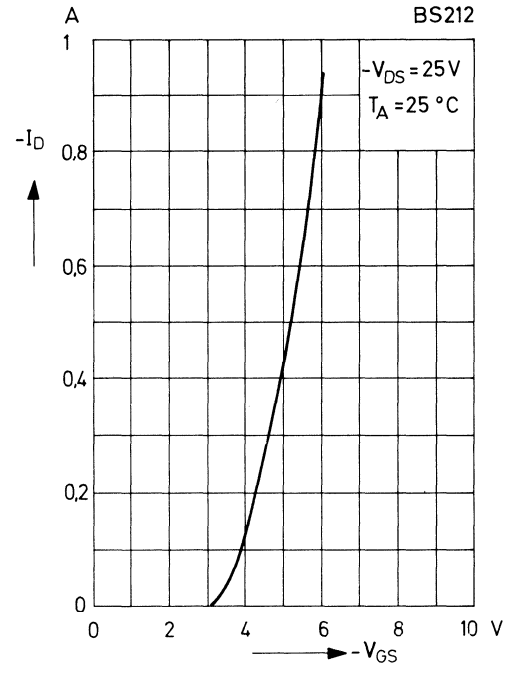


Drain-source current versus gate threshold voltage

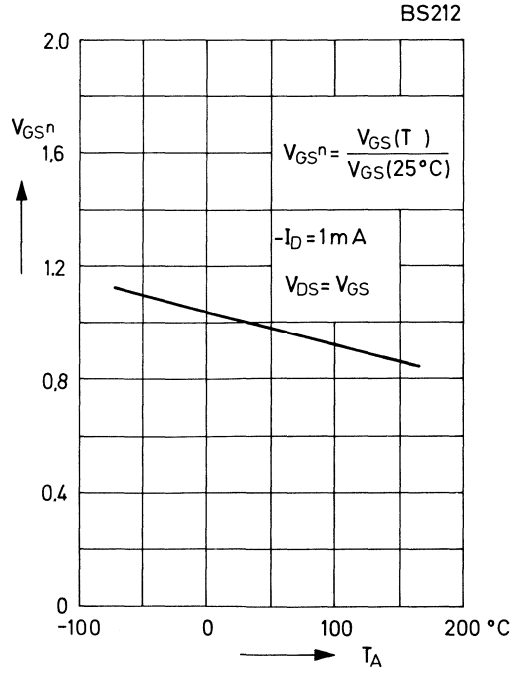


Drain current versus gate-source voltage

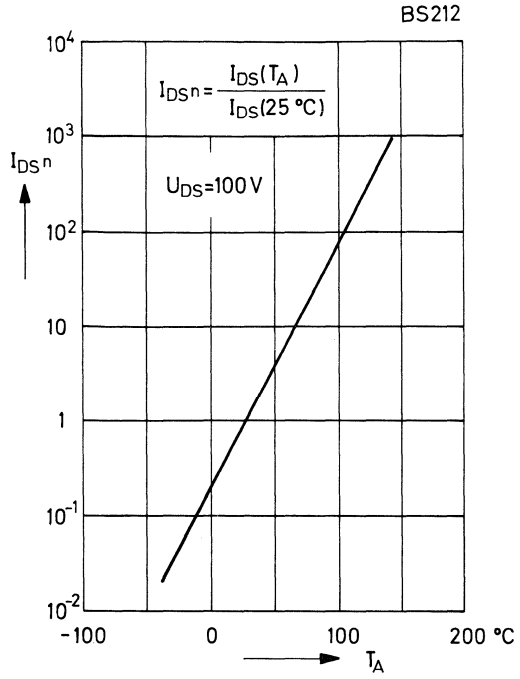
Pulse test width 80 μs; pulse duty factor 1%.



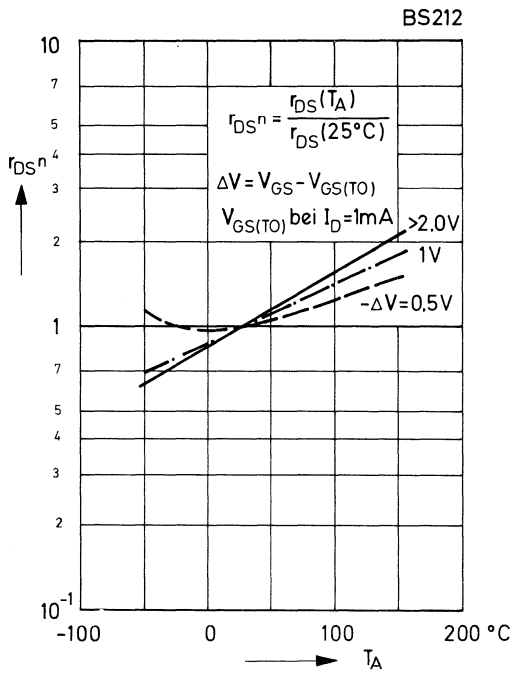
Normalized gate-source voltage versus temperature



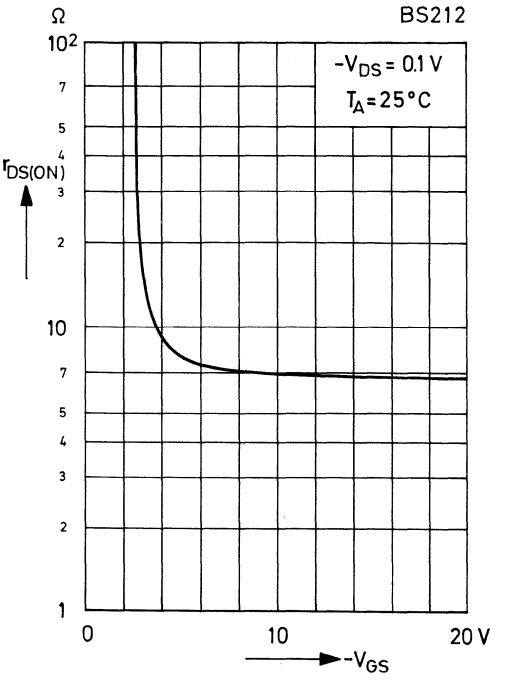
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

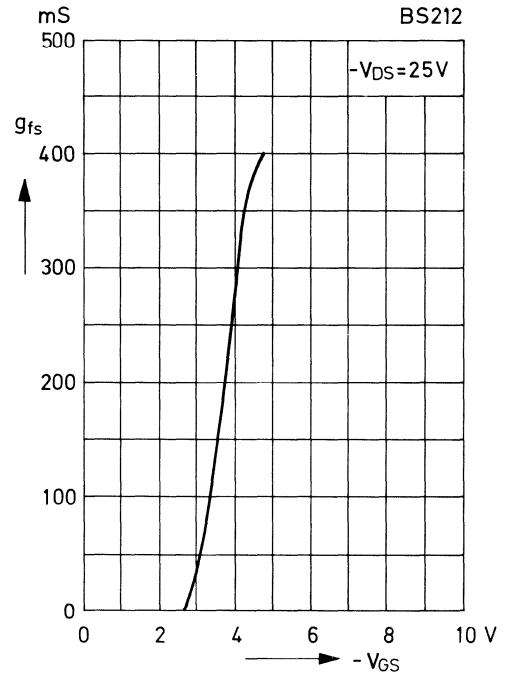


Drain-source resistance versus gate-source voltage



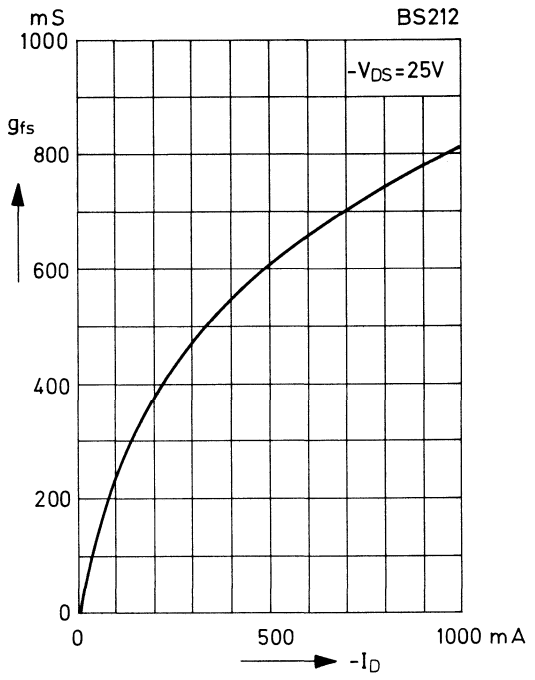
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%.

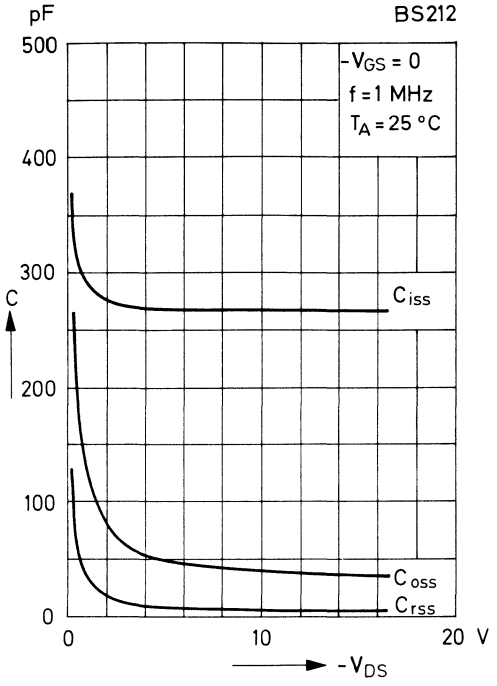


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%.



Capacitance versus drain-source voltage

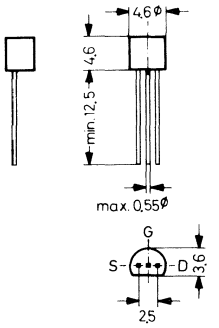


BS250

P-Channel Enhancement Mode VMOS Transistor

Features:
High input impedance
High speed switching
No minority carrier storage time
CMOS logic compatible input
No thermal runaway
No secondary breakdown

On special request this transistor is also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	45	V
Drain-Gate Voltage	$-V_{DGS}$	45	V
Gate-Source-Voltage (pulsed)	V_{GS}	±20	V
Drain Current (continuous)	$-I_D$	180	mA
Power Dissipation at T_C = 25 °C	P_{tot}	0.83[1)]	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	−55 . . . +150	°C
[1)] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case			

Inversediode

	Symbol	Value	Unit
Max. Forward Current (continuous) at T_{amb} = 25 °C	I_F	0.15	A
Forward Voltage Drop (typ.) at V_{GS} = 0, I_F = 0.15 A, T_j = 25 °C	V_F	0.85	V

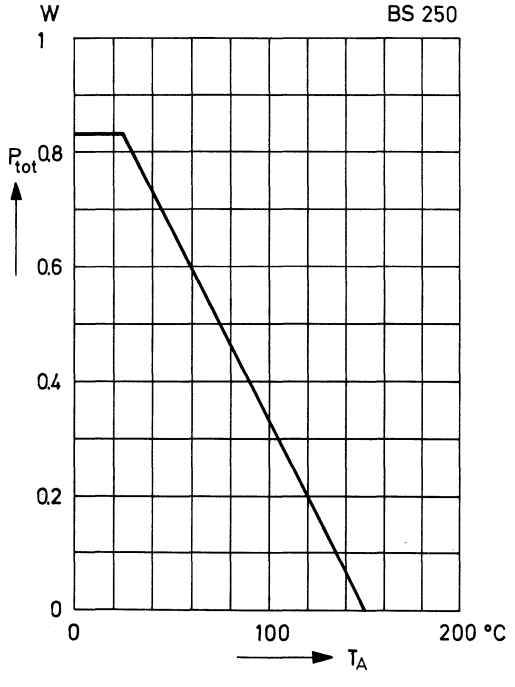
Characteristics at $T_j = 25\ °C$

	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $-I_D = 100\ \mu A$, $V_{GS} = 0$	$-V_{(BR)DSS}$	45	70	–	V
Gate Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D = 1$ mA	$V_{GS\,(TO)}$	1.0	2.8	3.5	V
Gate-Body Leakage Current at $-V_{GS} = 15$ V, $V_{DS} = 0$	$-I_{GSS}$	–	–	20	nA
Drain Cutoff Current at $-V_{DS} = 25$ V, $V_{GS} = 0$	$-I_{DSS}$	–	–	0.5	μA
Drain-Source On Resistance at $-V_{GS} = 10$ V, $-I_D = 0.2$ A	$r_{DS\,(ON)}$	–	9	14	Ω
Thermal Resistance Chip to Ambient Air	R_{thA}	–	–	150[1]	K/W
Forward Transconductance at $-V_{DS} = 10$ V, $-I_D = 0.2$ A, f = 1 MHz	g_m	–	150	–	mS
Input Capacitance at $-V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 MHz	C_{iss}	–	60	–	pF
Switching Times at $-V_{GS} = 10$ V, $-V_{DS} = 10$ V, $R_D = 100\ \Omega$					
Turn On Time	t_{on}	–	5	–	ns
Turn Off Time	t_{off}	–	25	–	ns

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

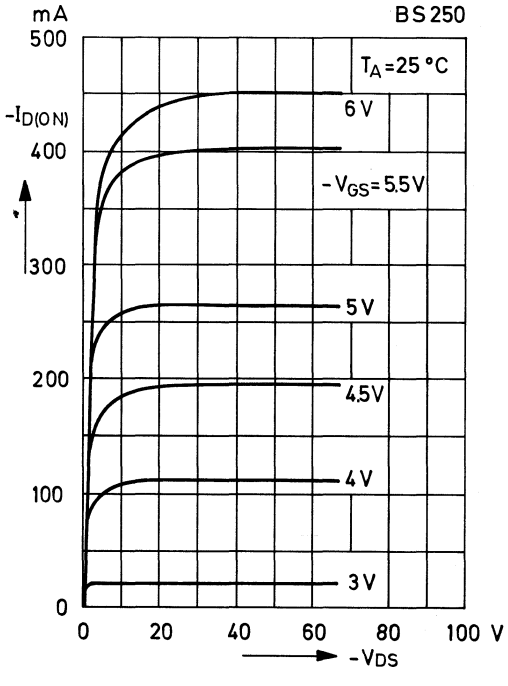
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case.



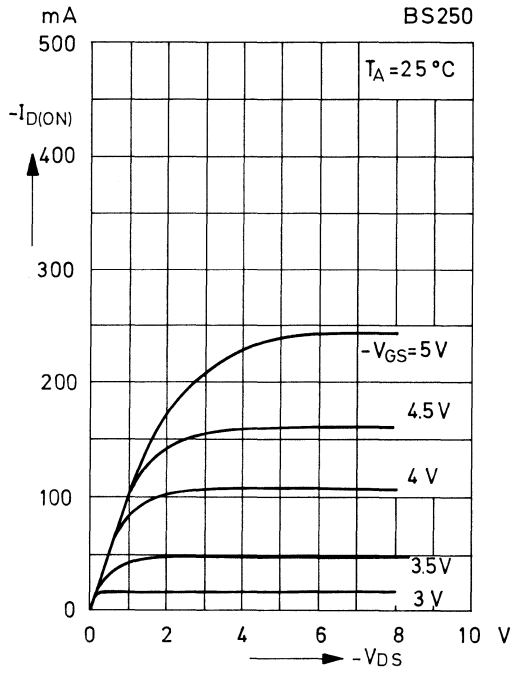
Output characteristics

Pulse test width 80 μs; pulse duty factor 1%.

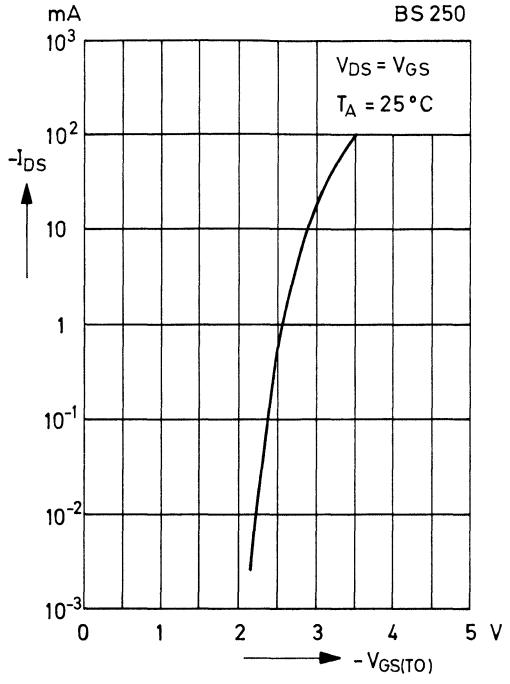


Saturation characteristics

Pulse test width 80 μs; pulse duty factor 1%.

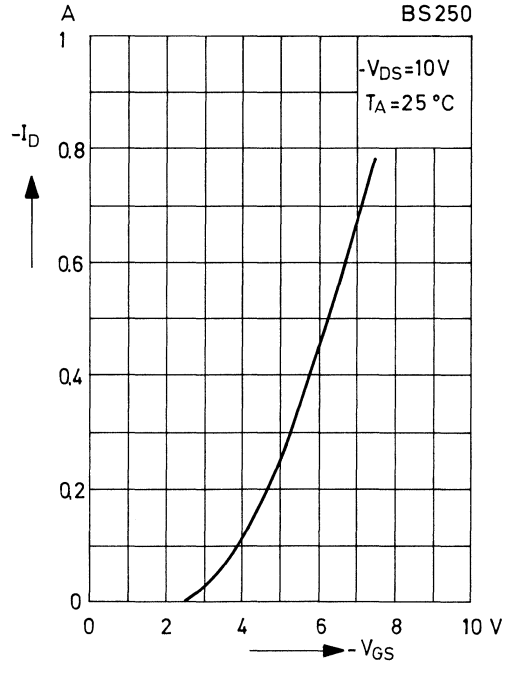


Drain-source current versus gate threshold voltage

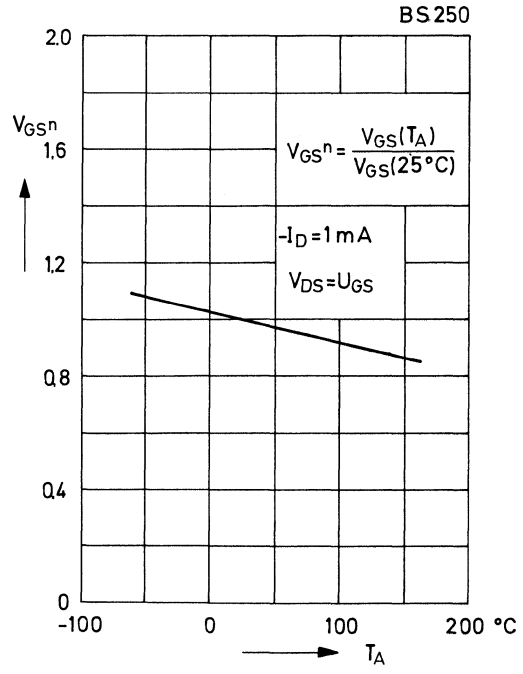


Drain current versus gate-source voltage

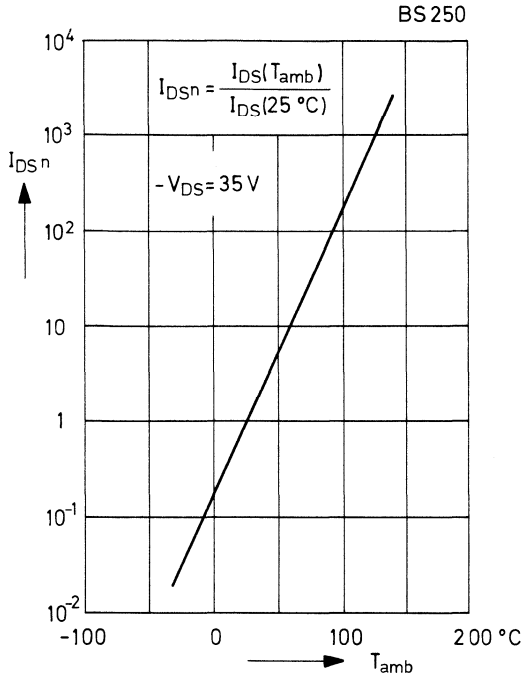
Pulse test width 80 μs; pulse duty factor 1%.



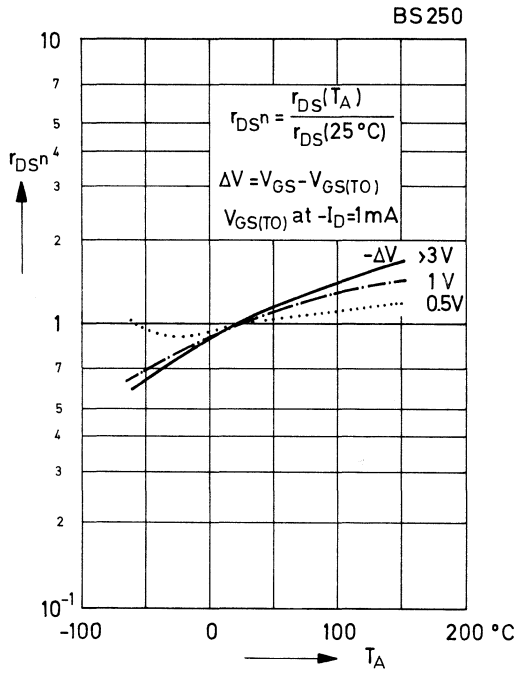
Normalized gate-source voltage versus temperature



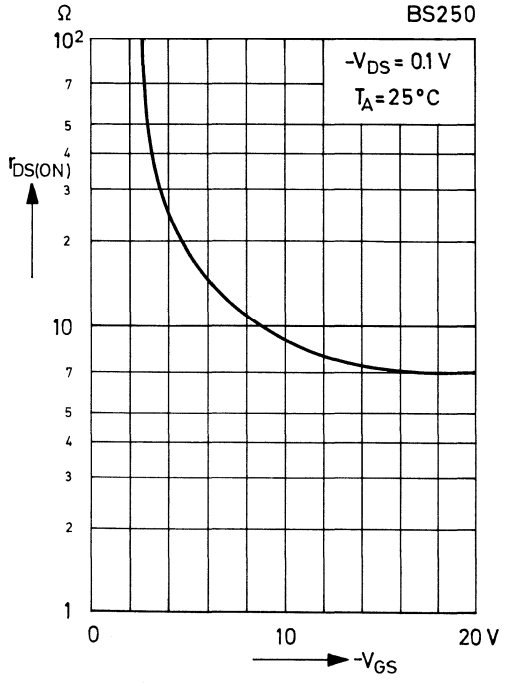
Normalized drain-source current versus temperature



Normalized drain-source resistance versus temperature

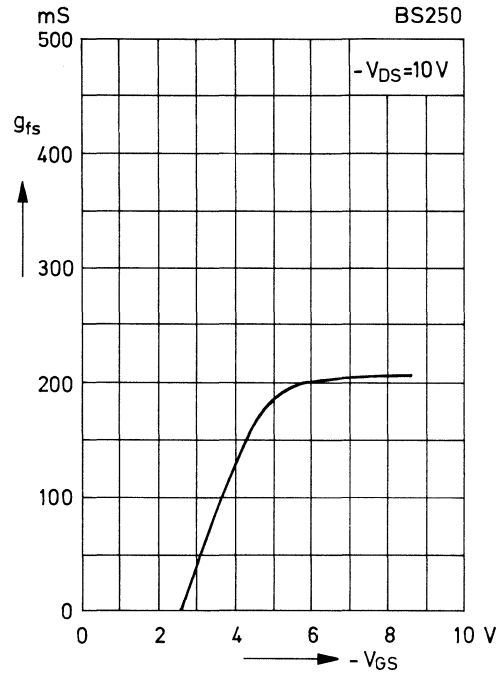


Drain-source resistance versus gate-source voltage



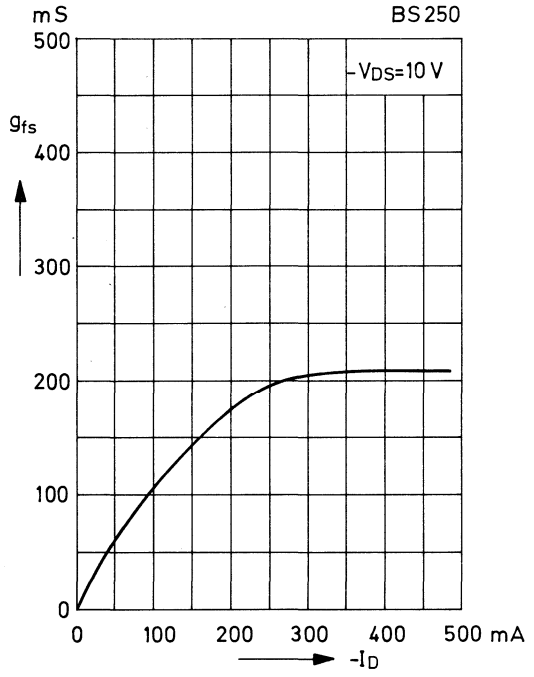
Transconductance versus gate-source voltage

Pulse test width 80 μs; pulse duty factor 1%.

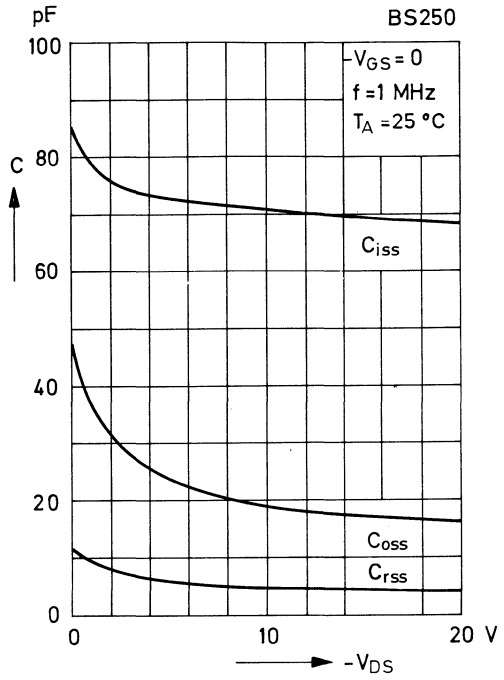


Transconductance versus drain current

Pulse test width 80 μs; pulse duty factor 1%.



Capacitance versus drain-source voltage



Semiconductors from ITT are worldwide available through your sales office/agent

Argentina
THIKO S.A.
Adolfo Alsina 1777
1088 Buenos Aires
Tel. (01) 45-65 63, 45-66 13,
45-71 15, 45-86 70
Fax (01) 40-38 11

Australia
CRUSADER
Electronic Components
Pty. Ltd.
73-81 Princes Highway
P.O. Box 14
St. Peters, N.S.W. 2044
Tel. (02) 516 38 55
Fax (02) 517 11 89

Austria
ITT MULTIcomponents
Akaziengasse 42
A-1234 Wien
Tel. (01) 69 45 17-0
Fax (01) 69 45 10

TRANSOHM
Vertriebsgesellschaft mbH
Kolbegasse 68
A-1232 Wien
Tel. (01) 6 10 66-0
Fax (01) 6 10 66-10

Belgium
ITT MULTIcomponents
Belgicastraat 2
B-1930 Zaventem
Tel. (02) 725 35 33
Fax (02) 725 41 35

Benelux
ITT Semiconductors Benelux
Maria Theresialei 7
B-2018 Antwerp
Tel. (03) 2 31 52 16
Fax (03) 2 31 56 42

Brazil
Top Tronic Tecnologia S.A.
Rua Dr. Migliano 1.110-7.0
and CJ705
05711 Morumbi – Sao Paulo, SP
Tel. (011) 842-9000
Fax (011) 842-3310

Bulgaria
SUNIMEX
Asparuh Str. 8
1000 Sofia
Tel. (2) 52 23 24
Fax (2) 54 26 86

Denmark
ITT MULTIkomponent
Naverland 29
DK-2600 Glostrup
Tel. (42) 45 66 45
Fax (42) 45 07 86

Egypt
Nagdy Engineering
8, El-Golf Street
P.O. Box 848 Maadi
Maadi – Cairo
Tel. (2) 350 - 07 66
Fax (2) 390 - 42 50

Finland
ITT MULTIkomponent
Tyopajakatu 5
SF-00500 Helsinki
Tel. (0) 73 91 00
Fax (0) 71 24 14

France
ITT Semiconductors France
157, rue des Blains
F-92220 Bagneux
Tel. (1) 45 47 81 81
Fax (1) 45 47 83 92

Germany
ITT INTERMETALL GmbH
Hans-Bunte-Strasse 19
P.O. Box 840
D-7800 Freiburg
Tel. (0761) 517-0

Hong Kong
DMF
Dek Mow Fung Tdg. Co. Ltd.
7th Floor, Block B
Chung Mei Centre
15–17 Hing Yip Street
Kwun Tong, Kowloon
Hong Kong
Tel. 797 20 78
Fax 790 60 62

香港及中国
德茂丰有限公司
香港九龙观塘兴业街十五至
十七号中美中心B座七楼
电话：797 2078
电传：30873 DMFA HX
图文传真：790 6062

Hungary
TELCON ELECTRONIC
Frankel Leo Utca 92. III. 15
H-1023 Budapest
Tel. (1) 369-430 + 368-316
Fax (1) 354-150

Iberia
ITT Semiconductors Iberia
c/o SWF Auto Electric
Ctra. Andalucia, Km. 10,3
E-28080 Madrid
Tel. (1) 7 95 67 65
Fax (1) 7 97 13 35

India
Krishan C. Arora & Co.
N-122, Greater Kailash-I
P.O. Box 4218
New Delhi – 110048
Tel. (11) 641-1133
Fax (11) 646-5297

Israel
Radion Engineering Company Ltd.
4, Rothschild Boulevard
Tel Aviv 61012
Tel. (03) 65 61 51 to 65 61 53
Fax (03) 66 27 69

Italy
ITT Semiconductors Italy
Viale Milanofiori, E/5
I-20090 Assago (Mi)
Tel. (02) 82 470.1
Fax (02) 82 426.31

Japan
ITT Semiconductors
(Far East) Ltd.
P.O. Box 21
Sumitomo Building
Shinjuku-ku
Tokyo 163
Tel. (03) 33 47-88 81
Fax (03) 33 47-88 44

Korea
Soei Korea Incorporation
Room 406, Shinhan Building
45-11, Yeoeido-Dong
Youngdeungpo-ku
Seoul
Tel. (02) 784-30 46...8
Fax (02) 785-34 07

Netherlands
ITT MULTIcomponents
Chroomstraat 28
NL-2718 RR Zoetermeer
Tel. (079) 613-161
Fax (079) 613-169

Nedis B.V.
Koningskampen 6
NL-5321 JK Hedel
P.O. Box 70
NL-5320 AB Hedel
Tel. (04199) 10 55
Fax (04199) 11 95

SPOERLE ELECTRONIC
Postbus 8820
NL-5605 LV Eindhoven
Tel. (040) 54 54 30
Fax (040) 53 55 40

Norway
ITT MULTIkomponent
Nedre Kaldbakkvei 88
N-1081 Oslo 10
Tel. (02) 32 12 70
Fax (02) 32 51 20

Portugal
SMP
Semiconductores e Electronica
de Portugal
Sao Gabriel – Cascais
P-2750 Cascais
Tel. (11) 2 84 50 22 + 2 84 55 22
Fax (11) 2 86 62 94

Scandinavia
ITT Semiconductors
Scandinavia
Naverland 29
DK-2600 Glostrup
Tel. (42) 45 18 22
Fax (42) 45 15 34

Singapore
ITT Semiconductors
(Far East) Ltd.
Representative Office
150 Orchard Road # 07-13
Orchard Plaza
Singapore 0923
Tel. 732 65 66
Fax 737 73 92

South Africa
STC Components (Pty.) Ltd.
Van Dyk Road
P.O. Box 1882
Boksburg 1460, Transvaal
Tel. (011) 899-61 11
Fax (011) 892-46 09

Spain
Sagitrón
Corazón de Maria, 80
E-28002 Madrid
Tel. (1) 416-9261
Fax (1) 416-8652

AKTA SPAIN, S.A.
Roger de Lluria No. 155 Enl. 1
E-08037 Barcelona
Tel. (3) 218-4949 + 218-4696
Fax (3) 238-1011

Sweden
ITT MULTIkomponent
Ankdammsgatan 32
P.O. Box 1330
S-17126 Solna
Tel. (08) 83 00 20
Fax (08) 27 13 03

Switzerland
ITT MULTIcomponents
Brandschenkestrasse 178
CH-8027 Zürich
Tel. (01) 2 04 61 11
Fax (01) 2 04 64 54

AKTA Multikomponent AG
Lättichstrasse 6
CH-6340 Baar
Tel. (042) 31 53 55
Fax (042) 31 70 76

Taiwan
WesTech Electronics, Inc.
5F, No. 197
Hoping E. Road, Sec. 1
Taipei, Taiwan/ROC
Tel. (02) 356-0620
Fax (02) 394-2047 + 394-205

United Kingdom
ITT Semiconductors U. K.
Rosemount House
Rosemount Avenue
West Byfleet
Surrey KT14 6LB
Tel. (0932) 33 61 16
Fax (0932) 33 61 48

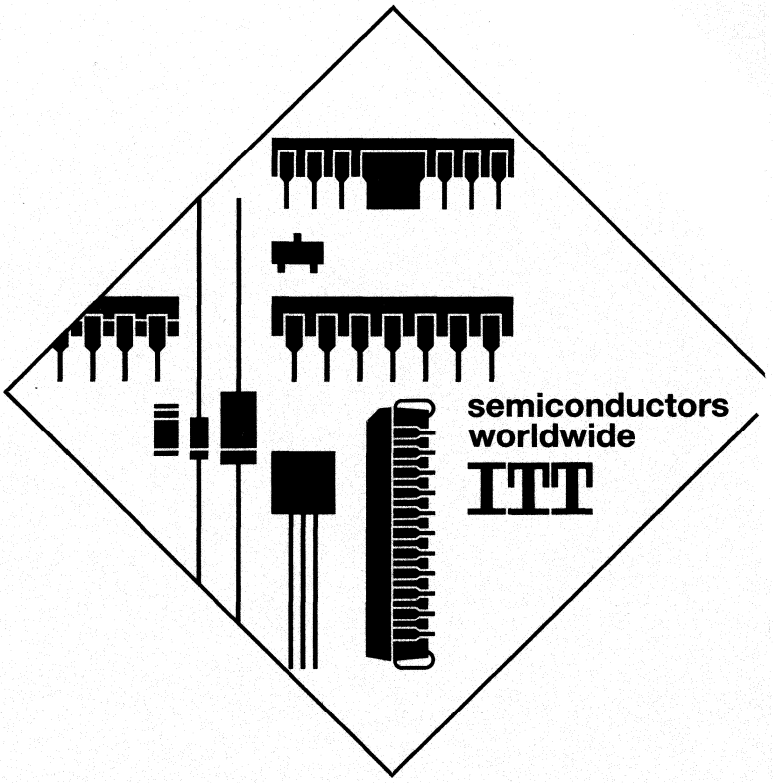
USA
U.S. Division
Sales Headquarters:

ITT Semiconductors
2500 West Higgins Road
Suite 735
Hoffman Estates, IL 60195
Tel. (312) 519-9610
Fax (312) 519-9615

Western Area:
ITT Semiconductors
2510 West 237th Street
Suite 208
Torrance, CA 90505
Tel. (213) 539-8051
Fax (213) 539-8044

Central Area:
ITT Semiconductors
909 West Maumee Street
Elmhurst Building
Angola, IN 46703
Tel. (219) 833-19 60
Fax (219) 665-28 11

Yugoslavia
Agens Representatives
Kamniška ulica 20
YU-61000 Ljubljana
Tel. (061) 31 27 44
Fax (061) 32 07 91



ITT Semiconductors Group
World Headquarters
INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-7800 Freiburg
Telephone (0761) 517-0
Telex 772715

Printed in Germany
Edition 1991/2
Order No. 6240-14-1E